

Compal Confidential

Model Name : ZIPS1

File Name : LA-A341P

BOM P/N:

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Stella M/B Schematics Document

Intel Shark Bay ULT Processor with DDR3L

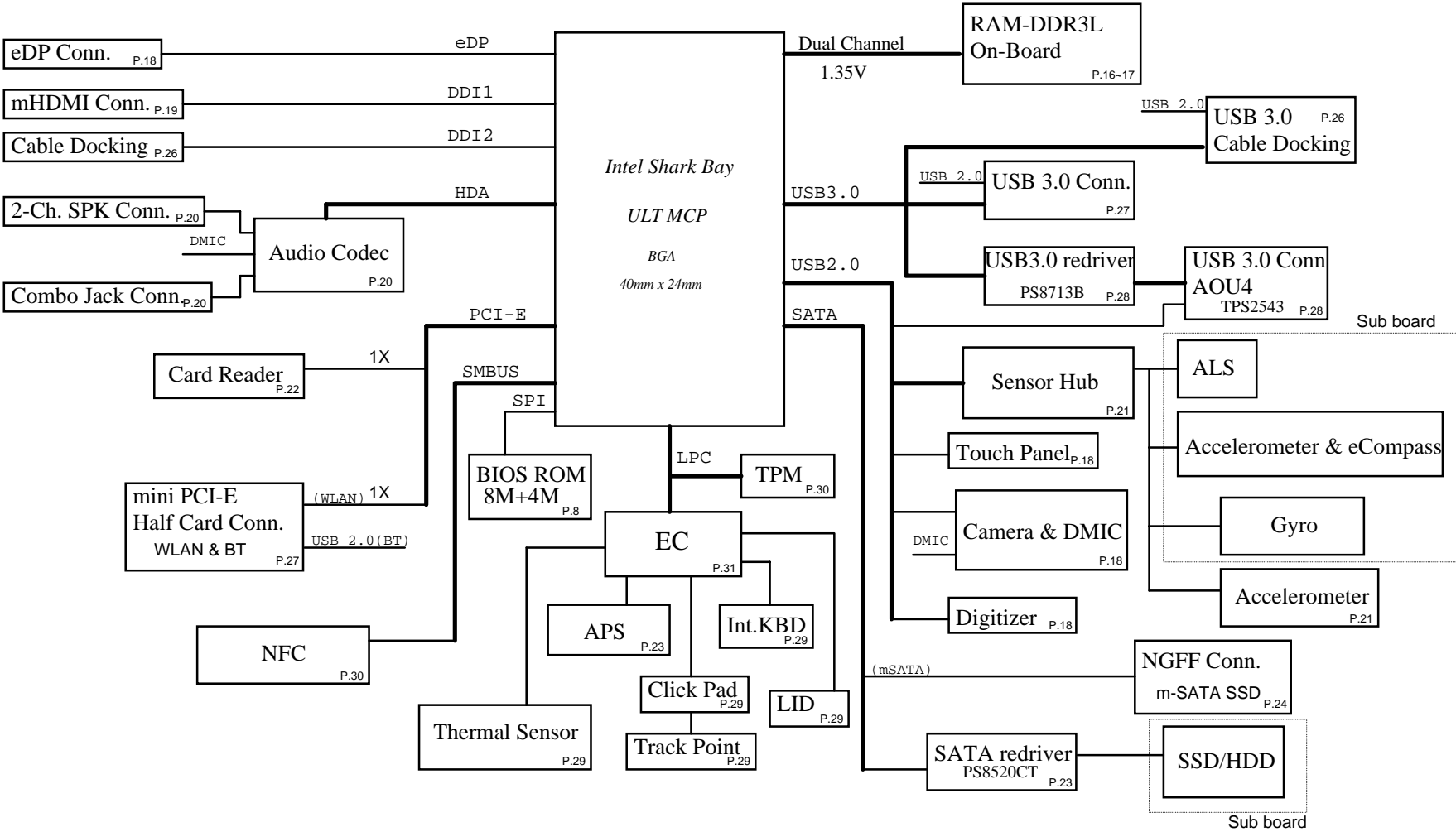
Rev. 1A_20130902A

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Model Name : ST-Note

File Name : Block Diagram



Voltage Rails

power plane	+B	+5VALW +3VALW	+1.35V	+5VS +3VS +1.5VS +VCCP +CPU_CORE	+3VM +1.05VM
State				+0.675VS +1.05VS	
S0	O	O	O	O	O M3 Supported
S3	O	O	O	X	O M3 Supported
S5 S4/AC	O	O	X	X	O M3 Supported
S5 S4/ Battery only (AOU Disable)	X	X	X	X	
S5 S4/AC & Battery don't exist (AOU Disable)	X	X	X	X	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

USB 2.0 Port Table

	USB 2.0	Port	3 External USB Port
		0	USB 3.0 Port + AOU (Left)
		1	USB 3.0 Port (Right)
		2	USB 3.0 Port (Docking)
		3	Mini Card (WLAN/BT)
		4	Touch Screen
		5	Camera
		6	Sensor Hub
		7	Digitizer

BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
EMI Mount	EMI@
dGPU	DIS@
Intel UMA	UMA@
AOAC	AOAC@
TPM	TPM@
SBA	SBA@
Non-SBA	NOSBA@
DRAM Option	DDR1@
Unpop	@
EMI Un-Mount	@EMI@

USB 3.0 Port Table

Port	
1	USB 3.0 Port (Left)
2	USB 3.0 Port (Right)
3	USB 3.0 Port (Docking)
4	

PCIe Port Table

Port	Lane	
1	/	
2		
3		WLAN
4		Cardreader
5	0	
	1	
	2	
	3	
6	0	
	1	
	2	
	3	

SATA Port Table

Port	
0	HDD
1	NGFF SSD
2	
3	

EC SM Bus1 address

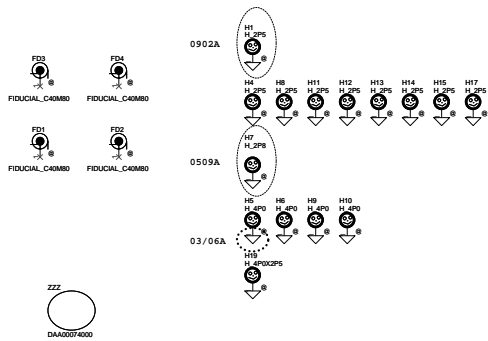
Device	Address	HEX
Smart Battery	0001 011X b	16H
Charger	0001 011X b	12H

EC SM Bus2 address

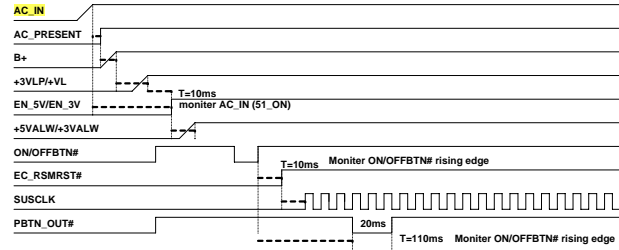
Device	Address	HEX
Thermal Sensor Fintek F75303M	1001_101xb	9AH
Synaptics Inter Touch Click Pad	0010_110xb	2CH

PCH SM Bus address

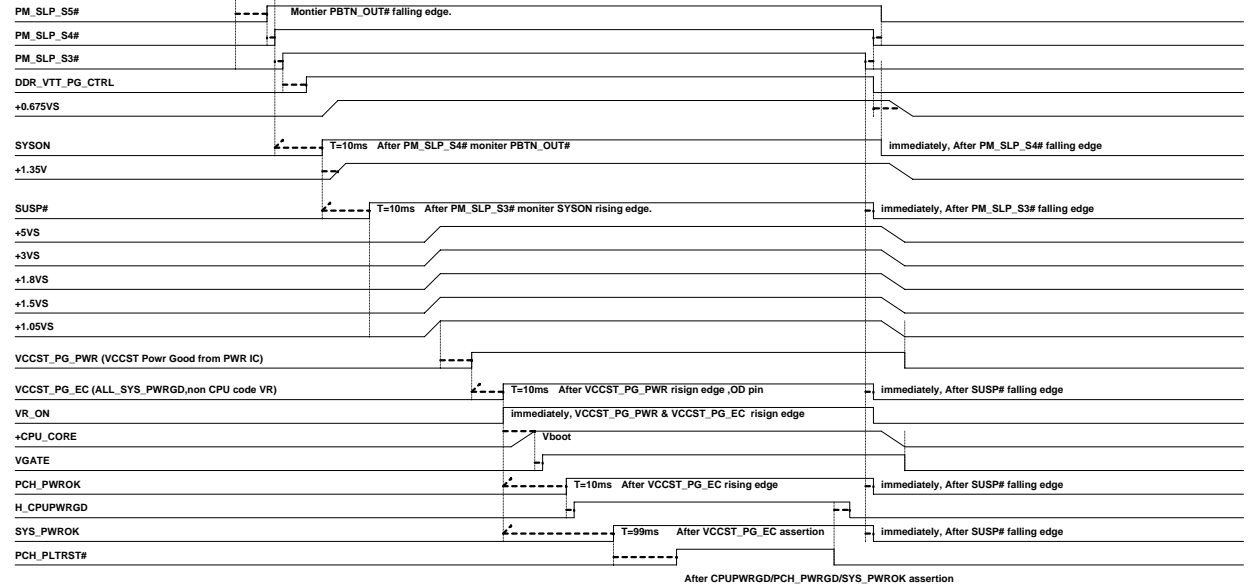
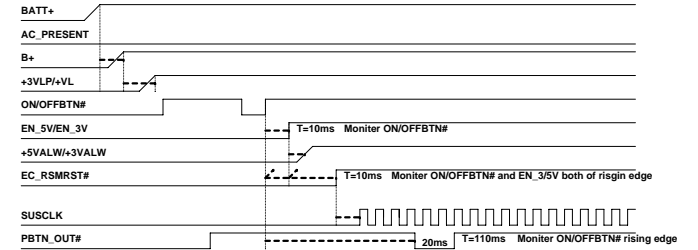
Device	Address	HEX
Security Rom	1010 100xb	A8H



[AC Mode]



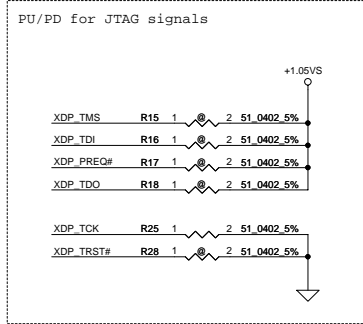
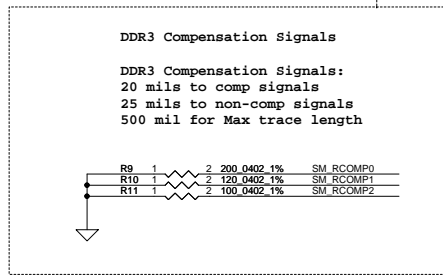
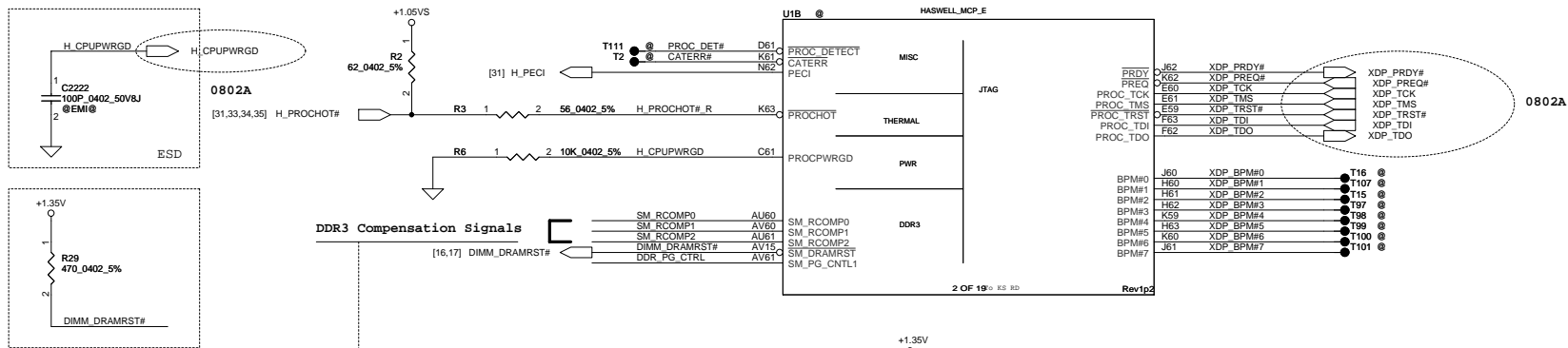
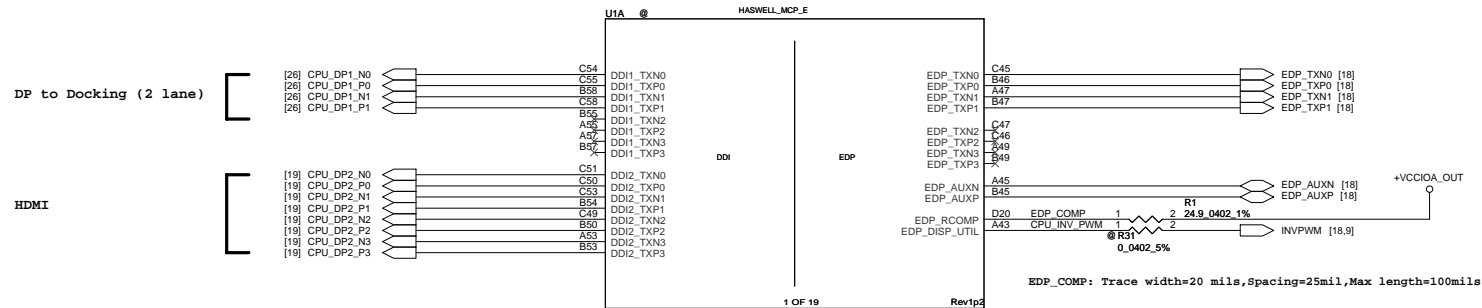
[DC Mode]



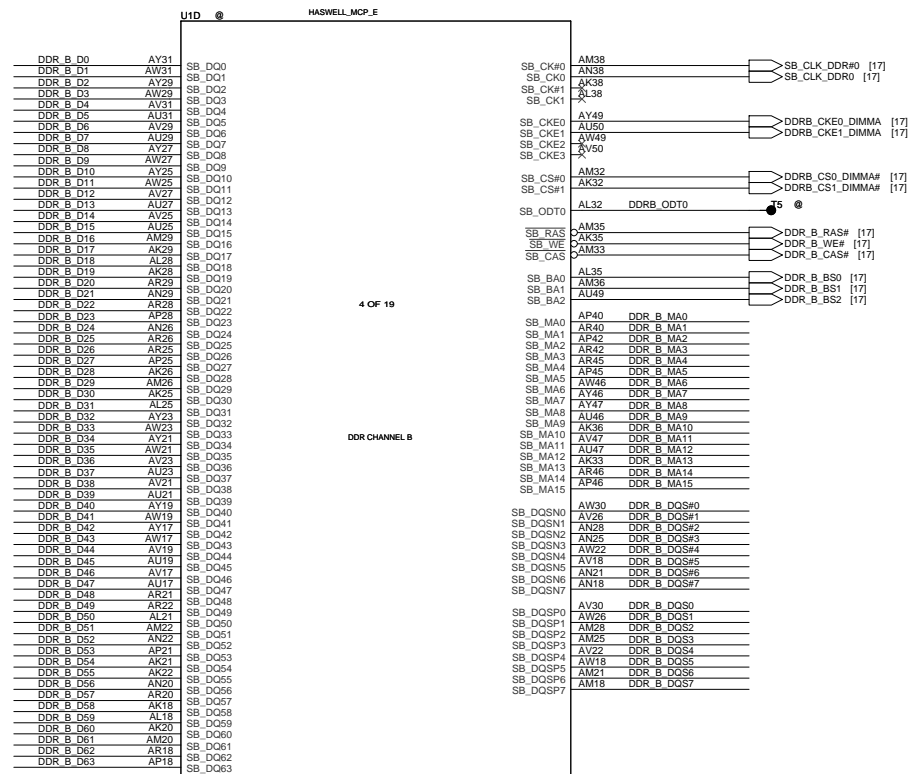
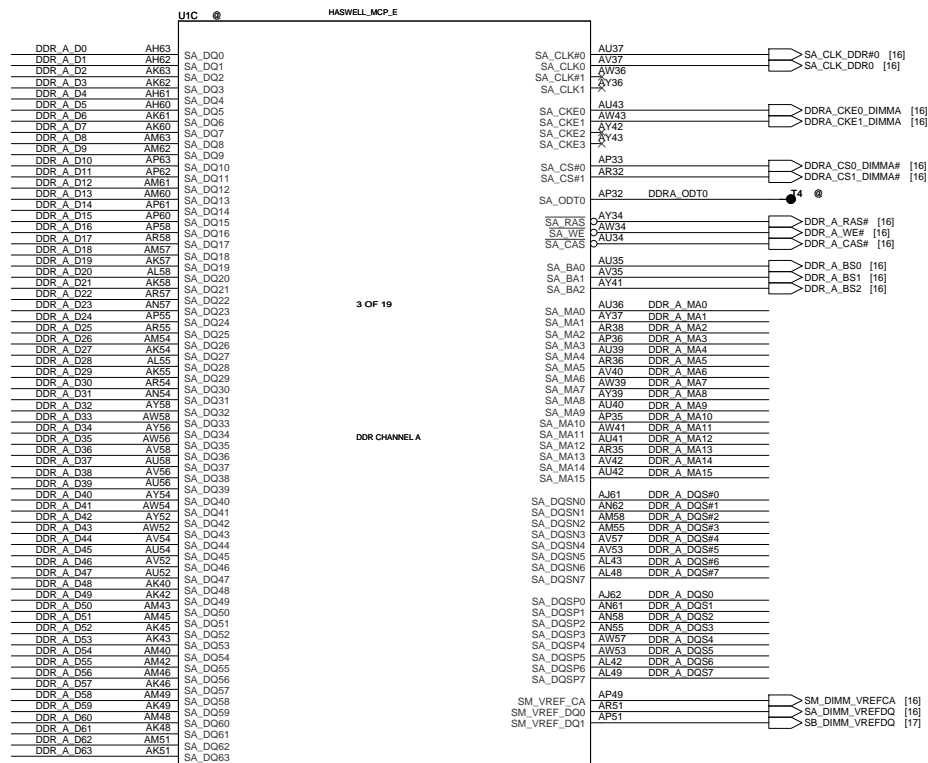
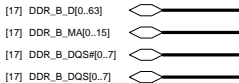
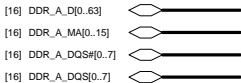
After CPUPWRGD/PCH_PWROK/SYS_PWROK assertion

RAM_ID3 GPIO46	RAM_ID2 GPIO47	RAM_ID1 GPIO48	RAM_ID0 GPIO49	RAM
0	0	0	0	HYNIX 4GB
0	0	0	1	SAMSUNG 4GB
0	0	1	0	MICRON 4GB
0	0	1	1	ELPIDA 4GB
0	1	0	0	SAMSUNG 8GB
0	1	0	1	ELPIDA 8GB
0	1	1	0	MICRON 8GB
0	1	1	1	HYNIX 8GB
1	0	0	0	TBD
1	0	0	1	TBD
1	0	1	0	TBD
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1	1	0	1	TBD
1	1	1	0	TBD
1	1	1	1	TBD

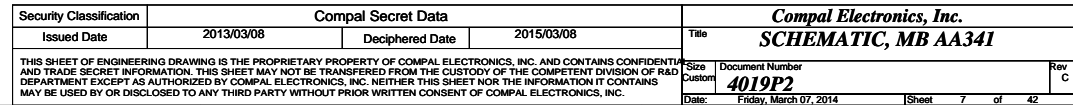
DDI/ MSIC/ XDP



Memory I/F



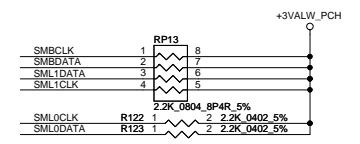
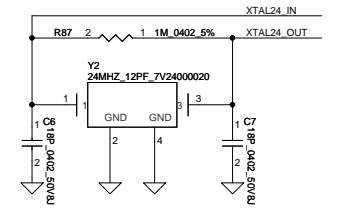
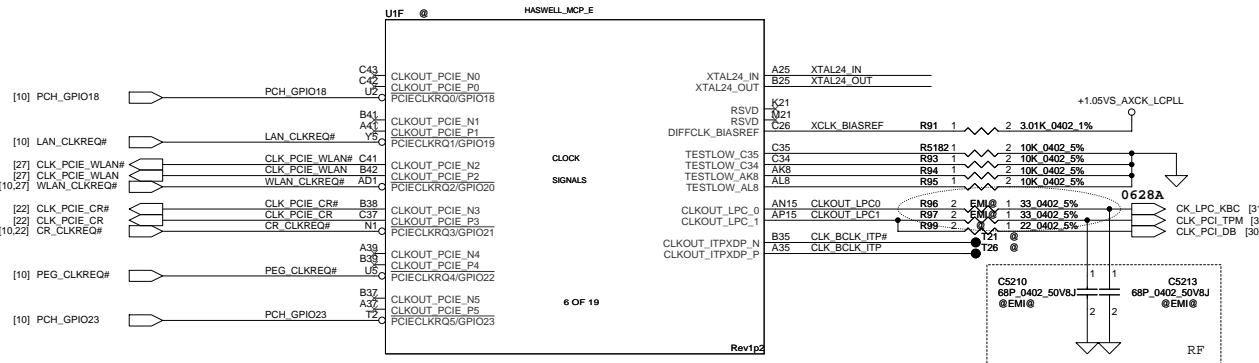
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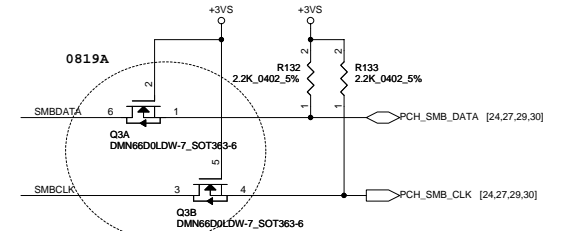
CLK/ SPI/ SMBUS

WLAN

Card Reader

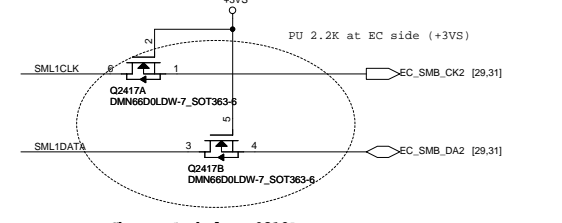


SMBus :SPD/PCIE/Security/TP/NFC



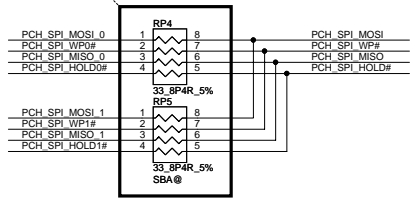
Change Symbol

SML1 Bus :EC/Sensors



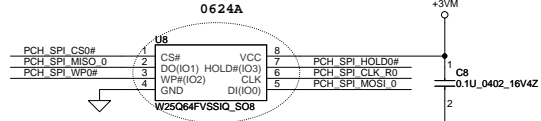
Change Symbol

SBA - 2 SPI Device = 33 ohm - P/N: SD309330A80
Non-SBA - 1 SPI Device = 15 ohm - P/N: SD300001P00



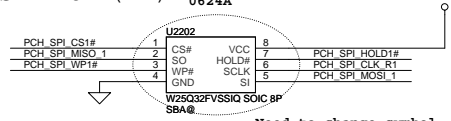
SPI ROM (8M)

SPI ROM 8MB
1st: SA000039A30 - Winbond
2nd: SA000046400 - E-ON
SPI ROM 4MB
1st: SA00003K820 - Winbond
2nd: SA00004LI00 - E-ON



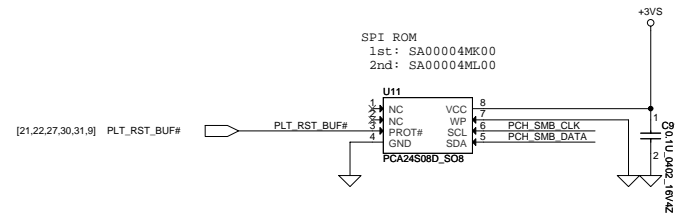
Need to change symbol

SPI ROM (4M)



Need to change symbol

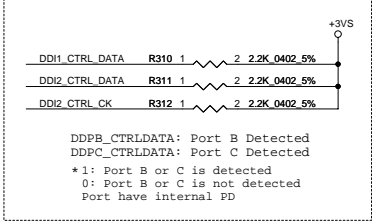
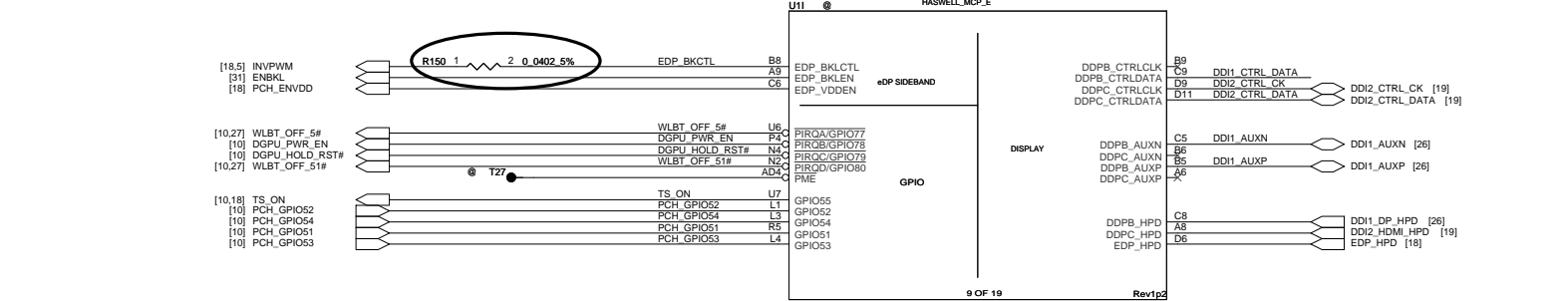
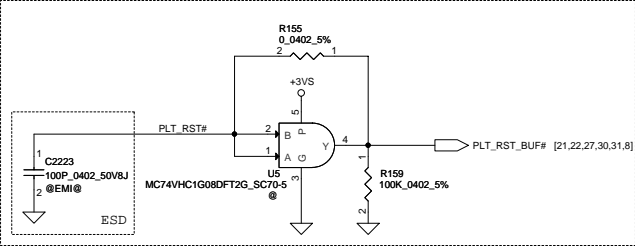
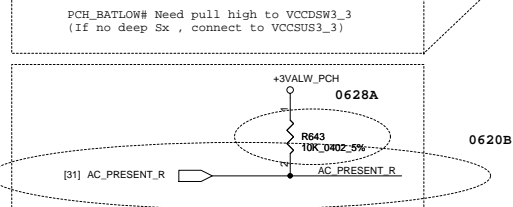
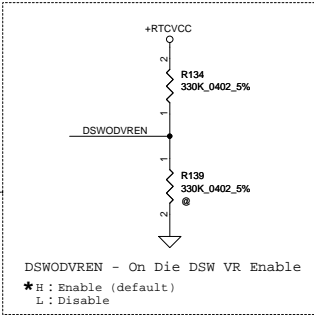
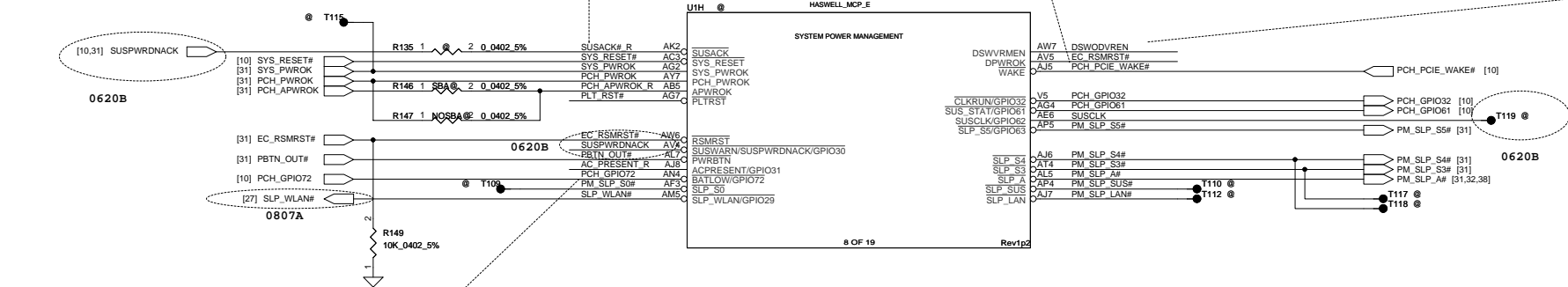
Security ROM



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PM/ GPIO/ DDI

Note: SUSACK# and SUSWRN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit.
CAN be NC ,if not support Deep Sx

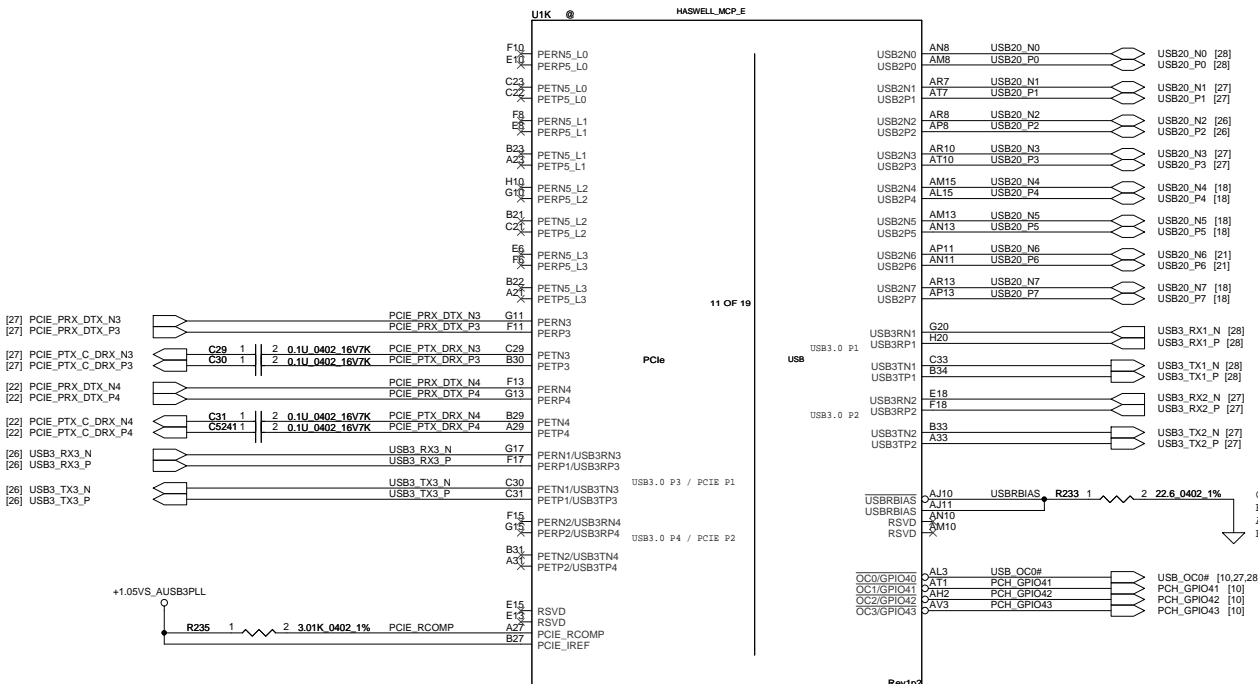


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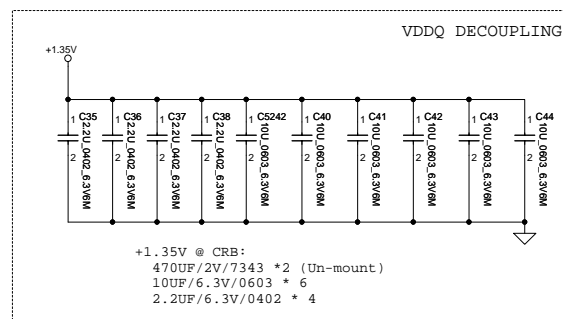
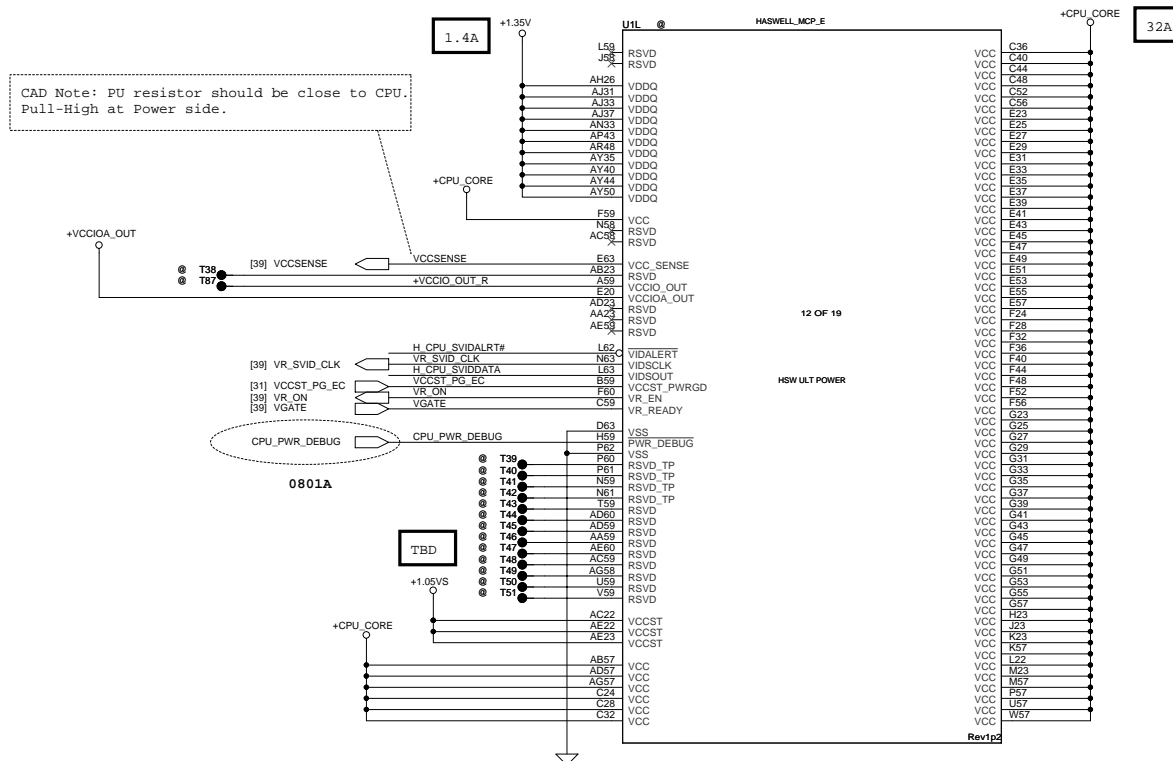
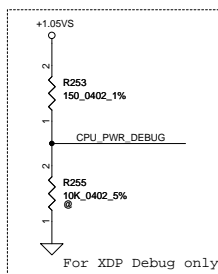
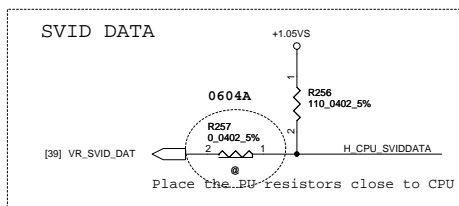
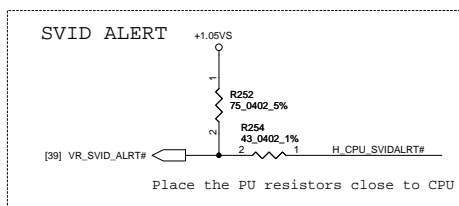
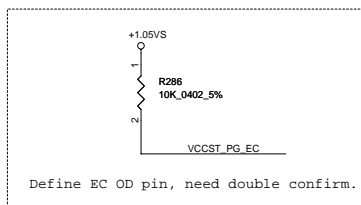
WLAN

Card Reader

USB 2/3 (Docking)



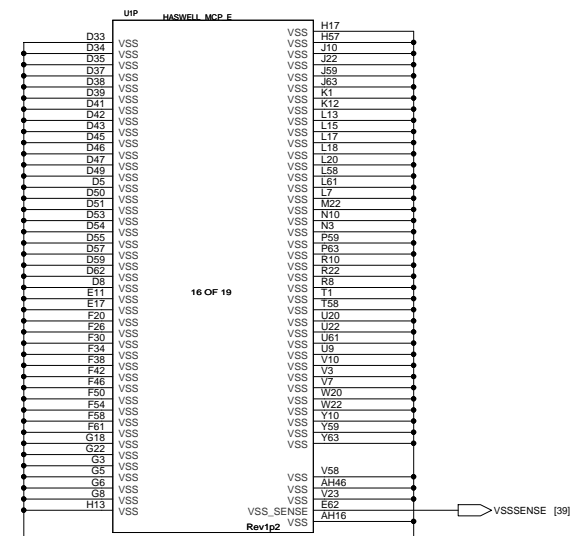
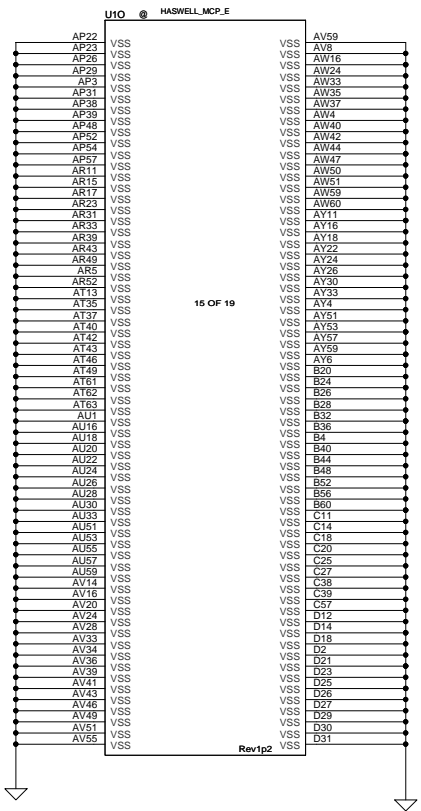
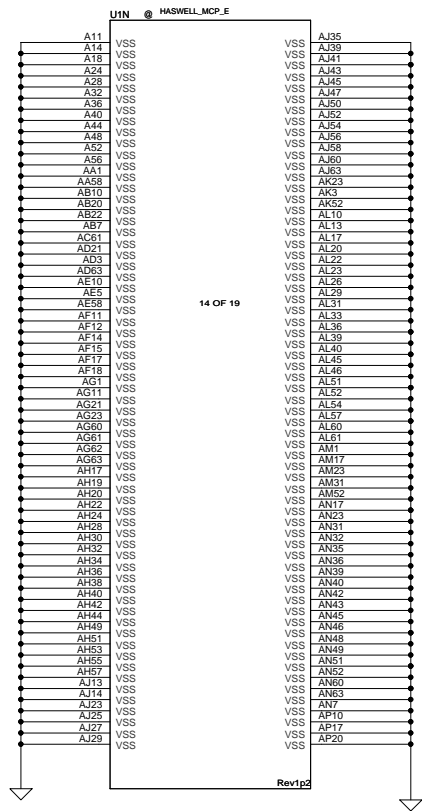
- USB2/3 (Left)
- USB2/3 IO (Right)
- USB2/3 IO (Docking)
- Mini Card(WLAN+BT)
- Touch Screen
- Camera
- Sensor Hub
- Digitizer
- USB2/3 (Left)
- USB2/3 (Right)

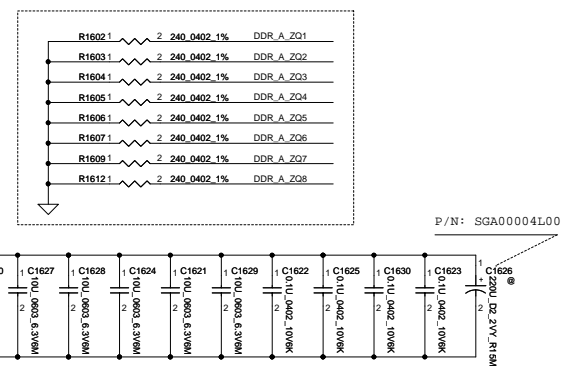
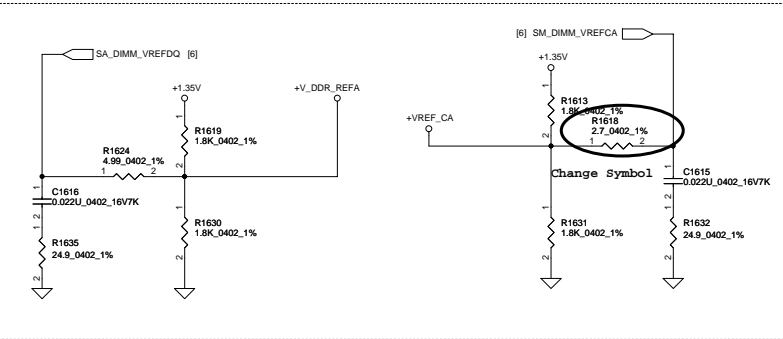


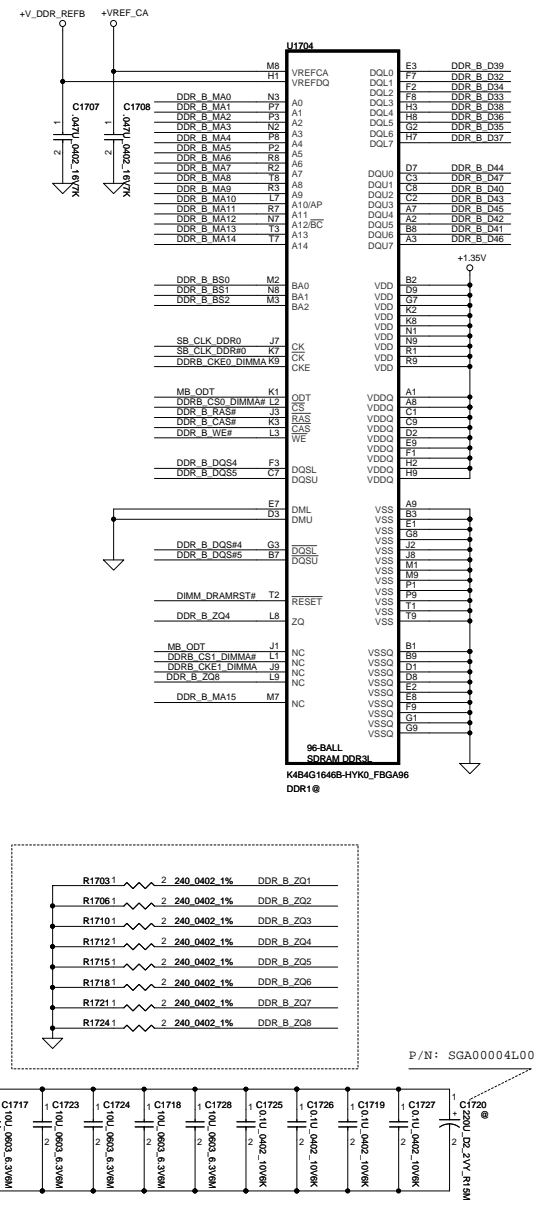
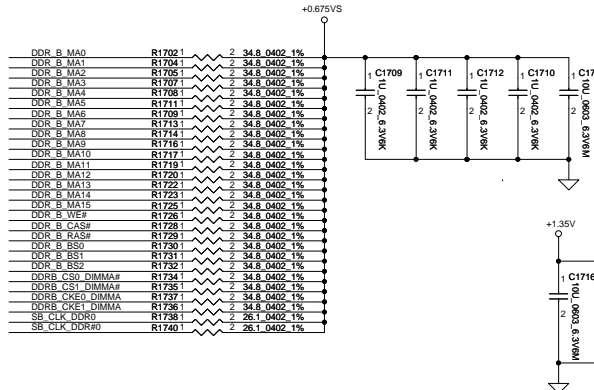
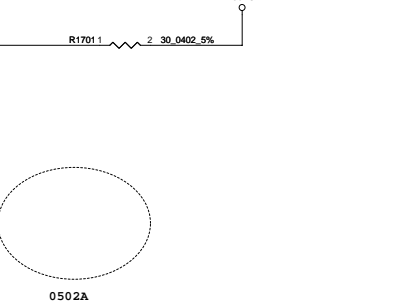
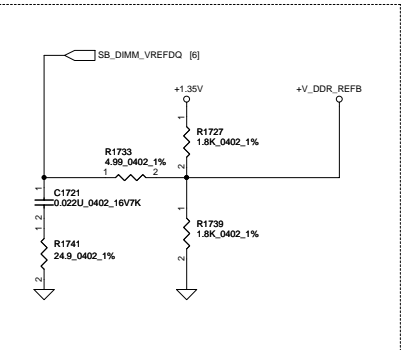
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[illegible]

GND





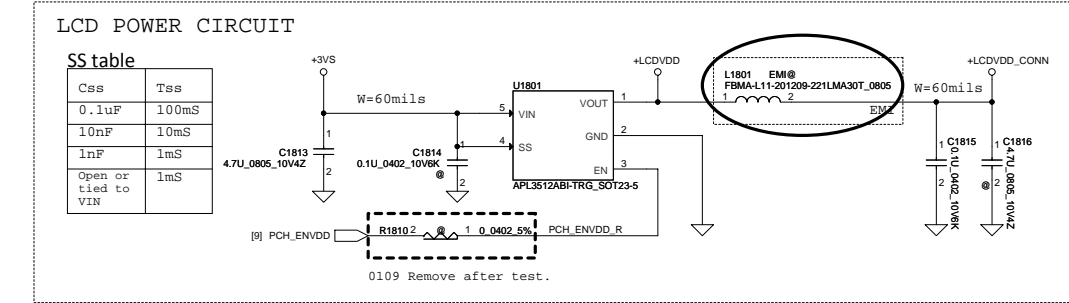
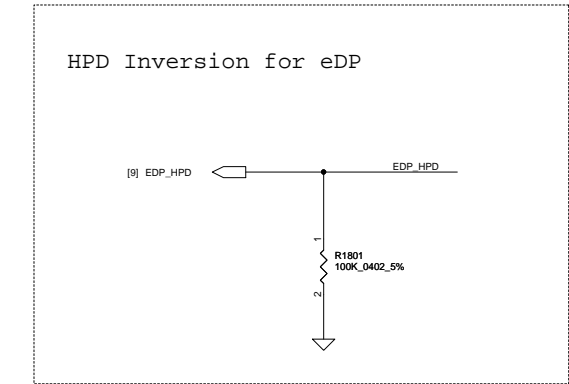
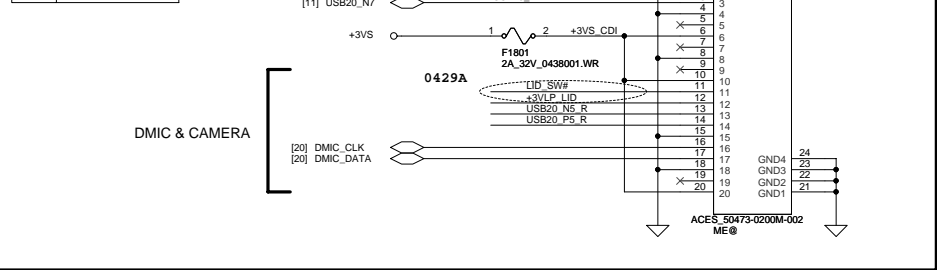


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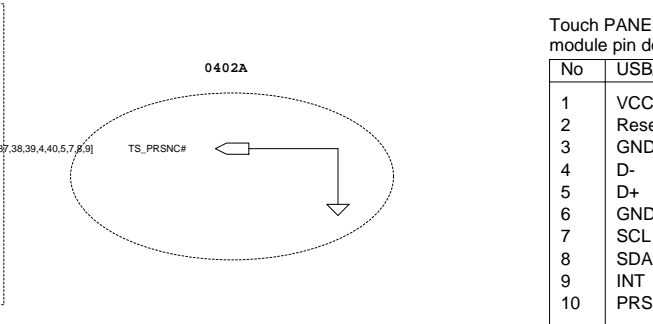
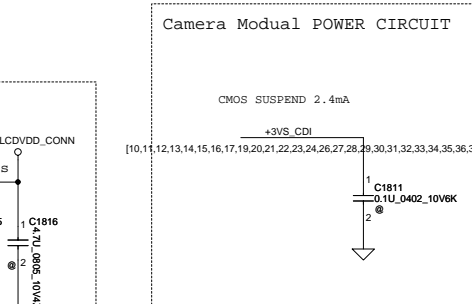
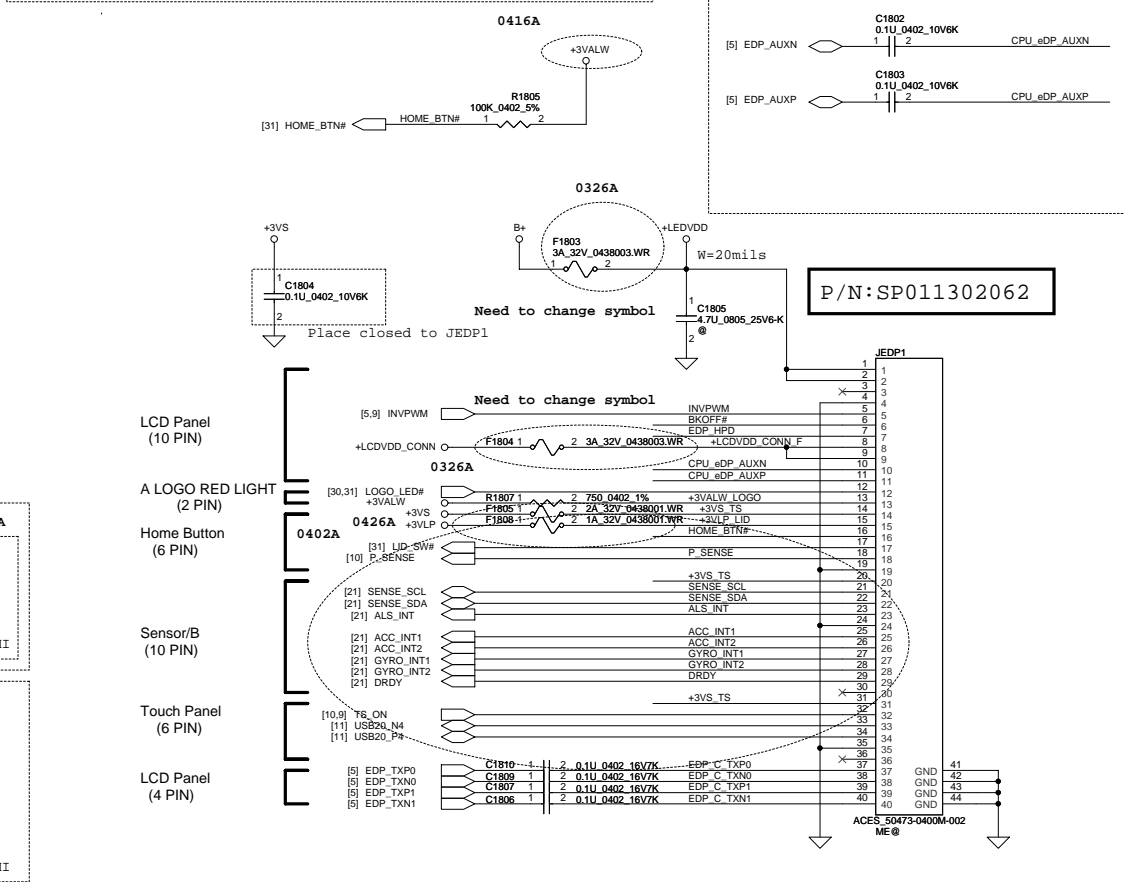
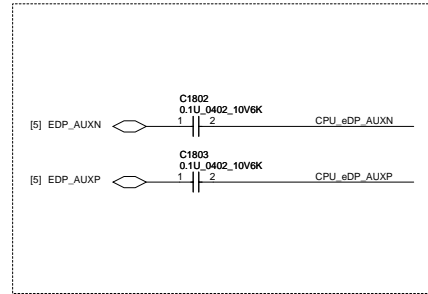
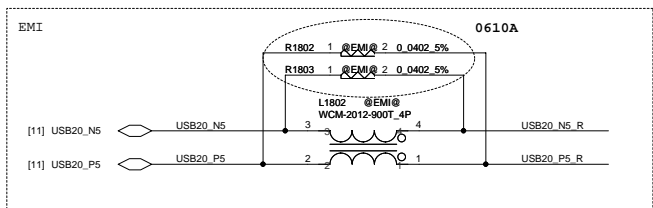
Digitizer & CMOS Conn

DMIC & CAMERA module pin define

No	SIGNAL
1	VCC (3.3V)
2	D-
3	D+
4	GND_CAM
5	GND_DMIC
6	MIC_C
7	MIC_D
8	MIC_VCC



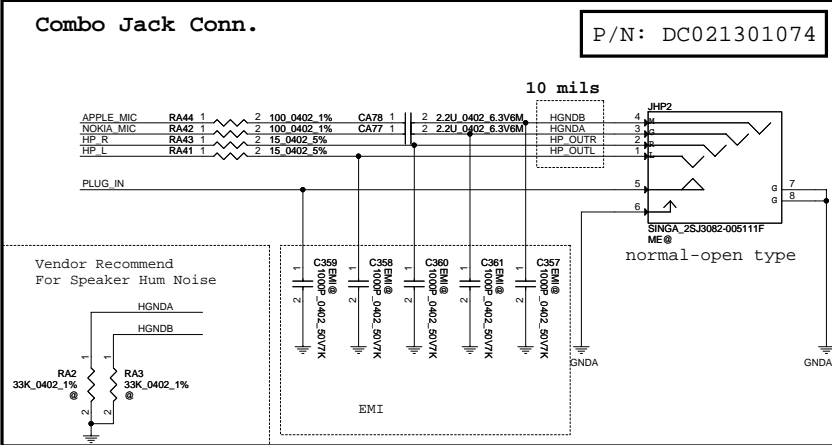
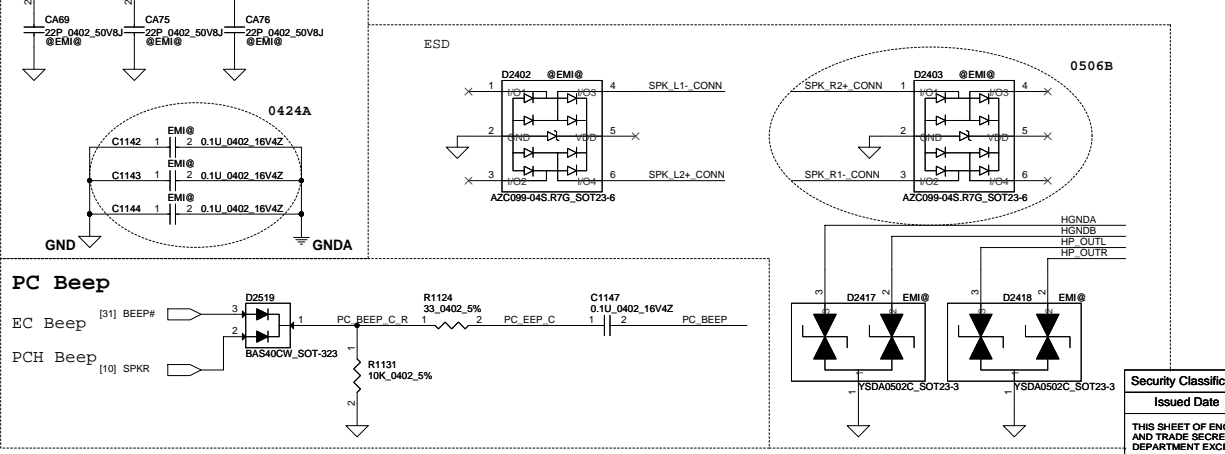
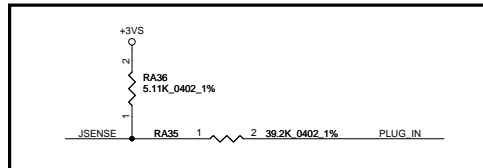
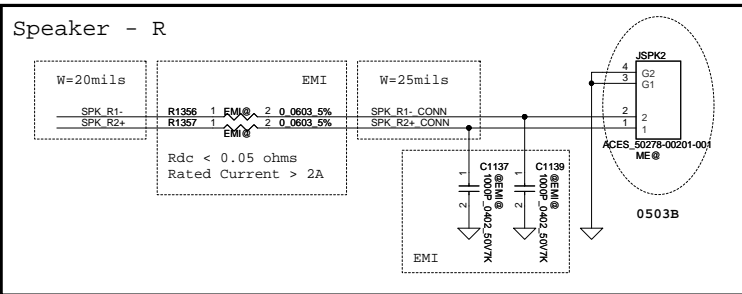
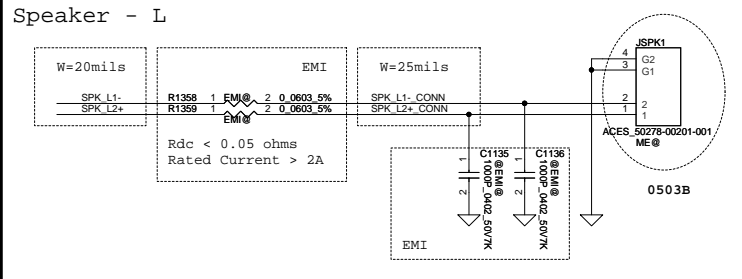
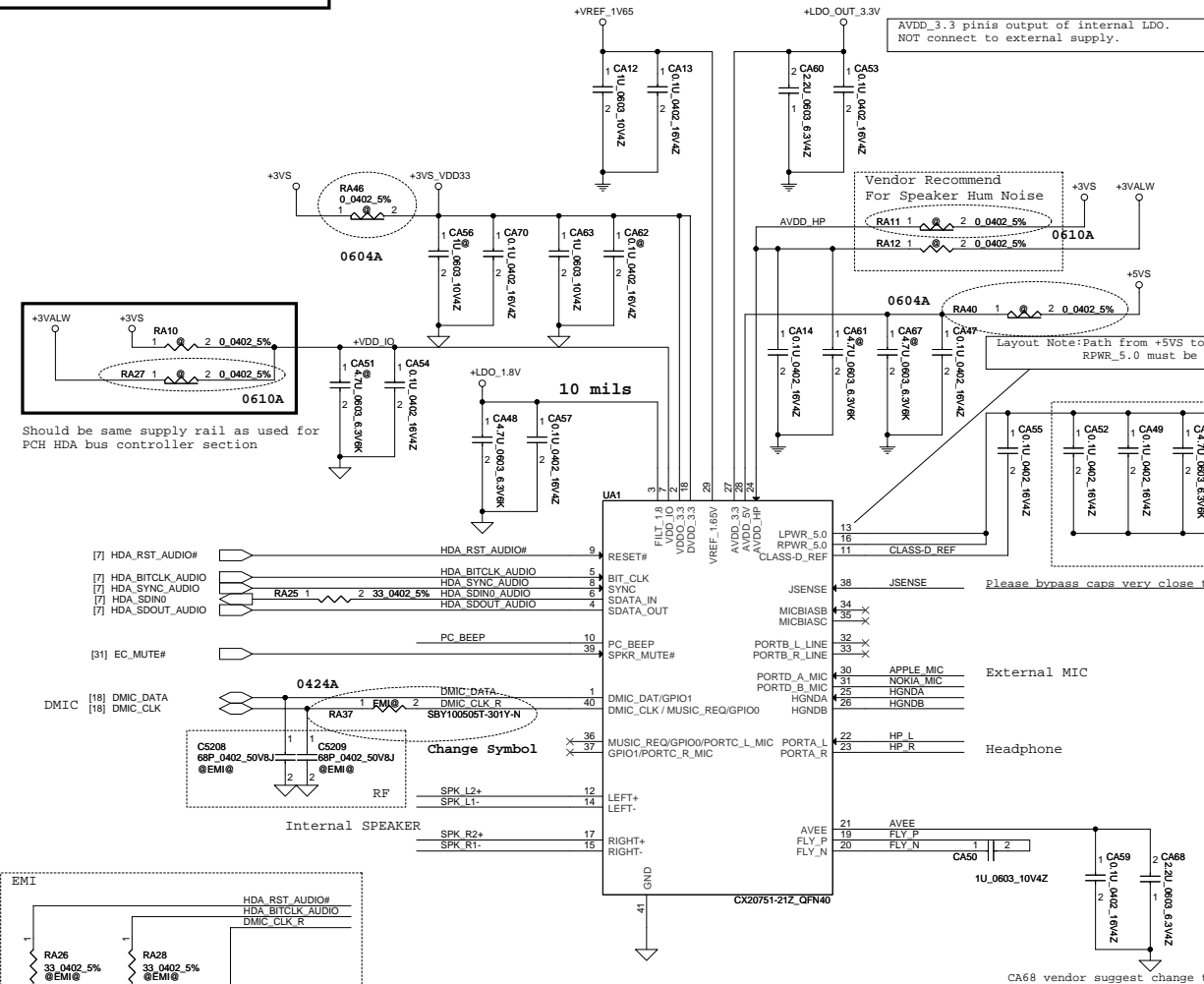
eDP Panel Conn



Touch PANEL module pin define

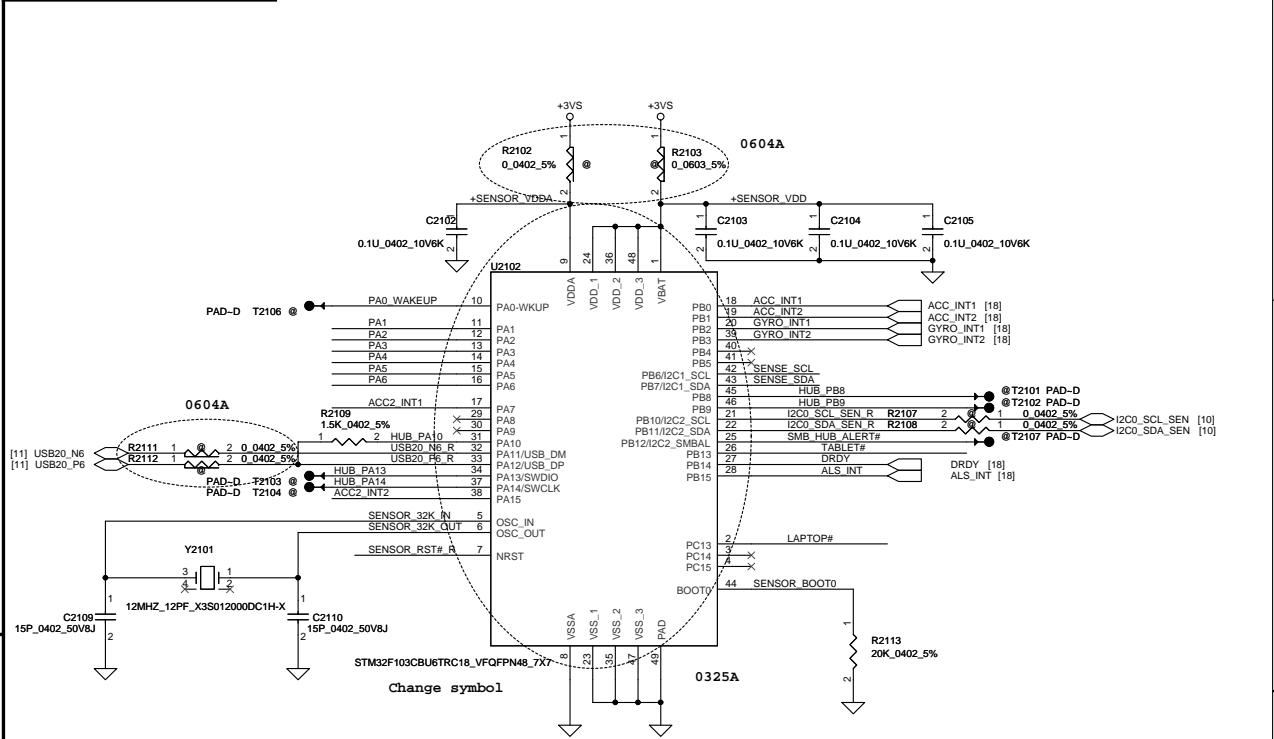
No	USB/I2C
1	VCC (3.3V)
2	Reset
3	GND
4	D-
5	D+
6	GND
7	SCL
8	SDA
9	INT
10	PRSENT

Audio CX20751

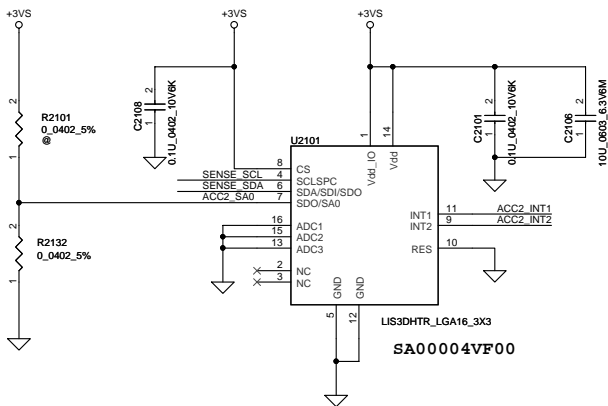


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				Document Number	4019P2
				Date	Friday, March 07, 2014
				Sheet	20 of 42

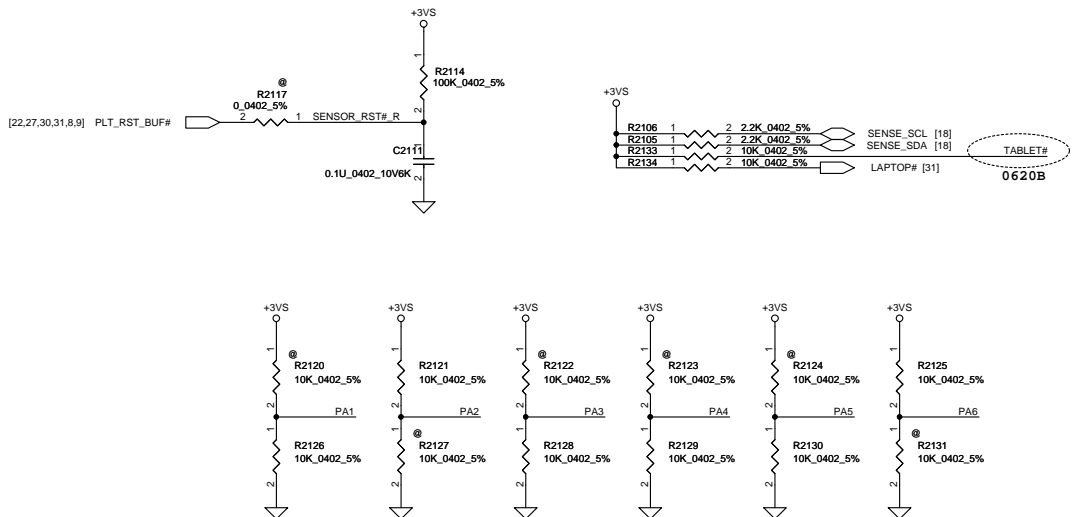
Sensor Hub



2nd G-sensor

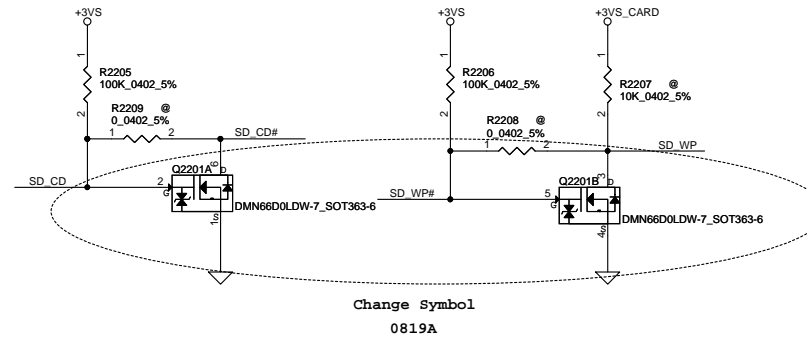
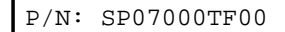


	ACC2_SA0
H	0x33h 0x32h
L	0x31h 0x30h



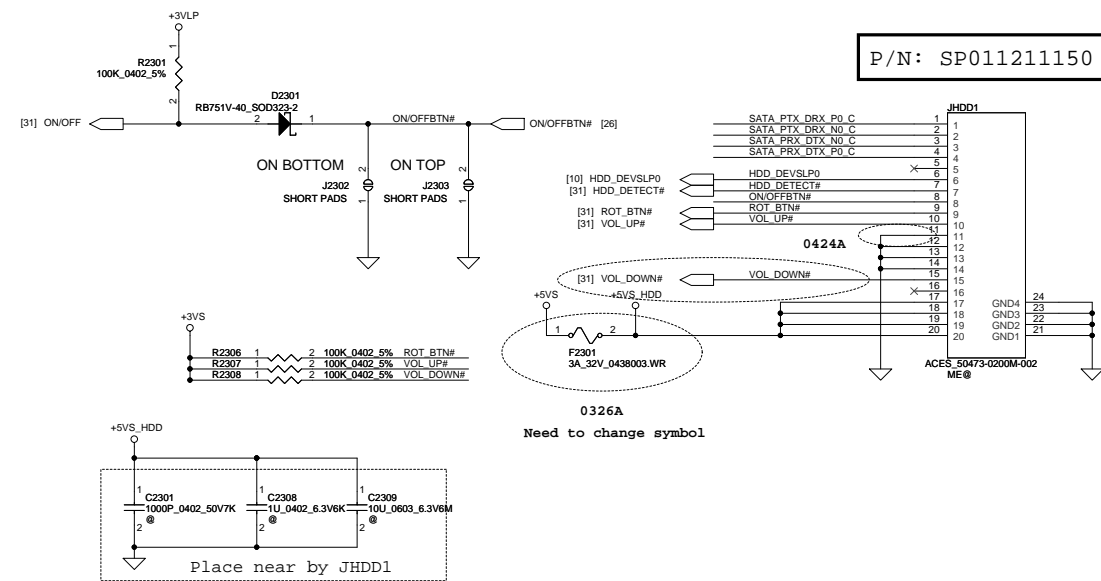
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				Date:	Friday, March 07, 2014	Sheet

Close to Pin 27

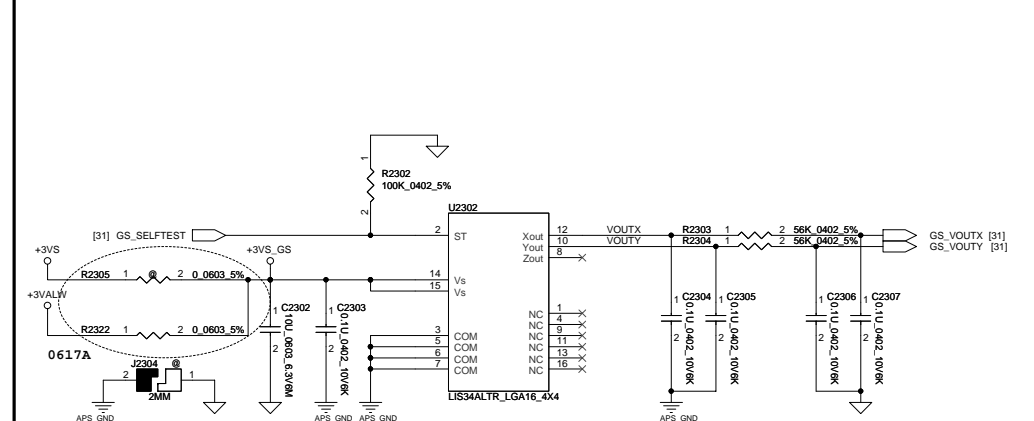


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				Date:	Friday, March 07, 2014
				Sheet	22 of 42

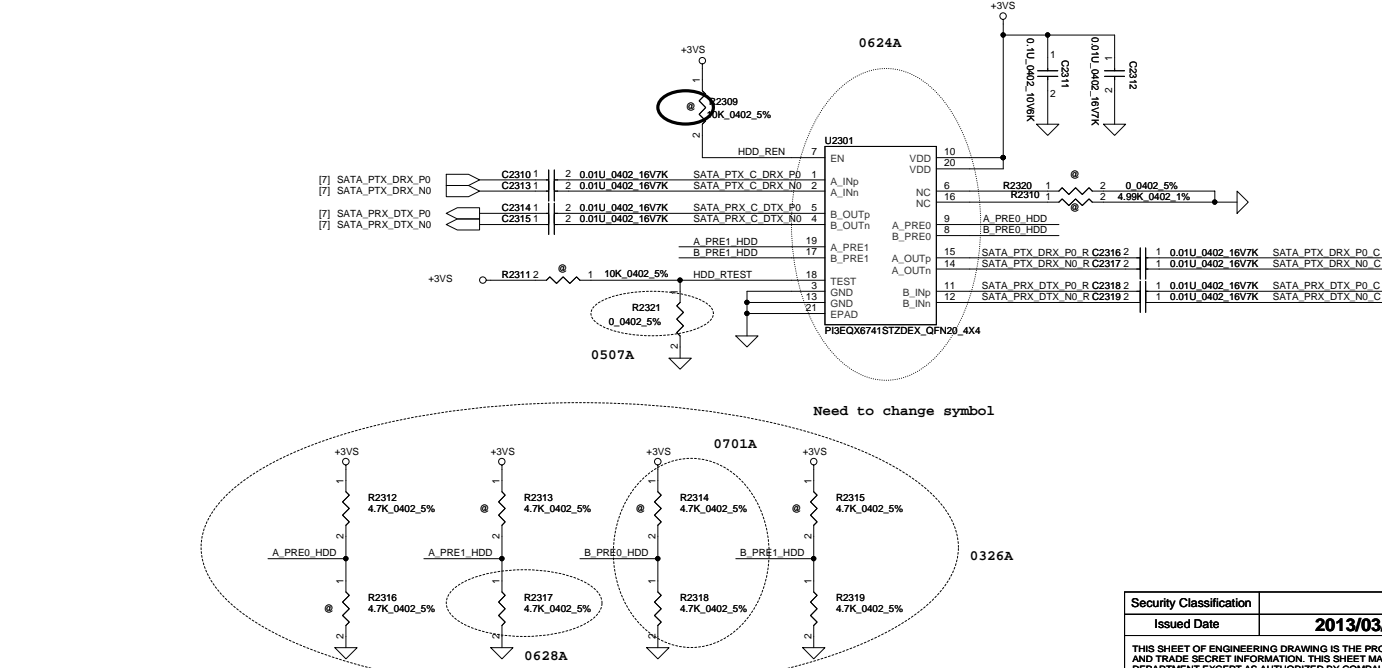
SATA HDD WTB Conn



APS G-Sensor



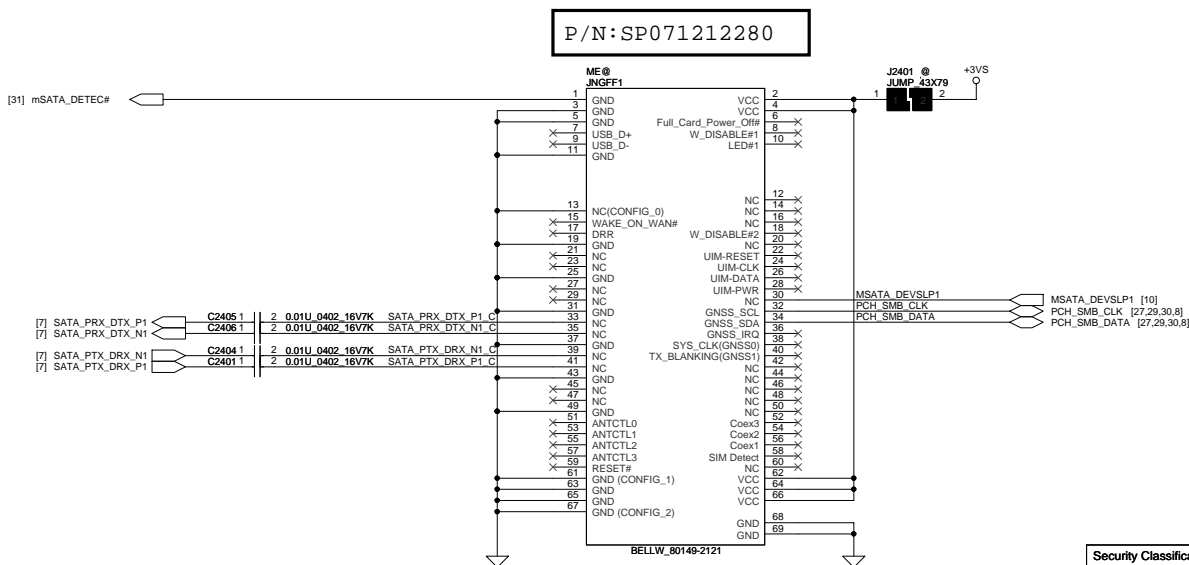
HDD SATA Redriver



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NGFF SATA Redriver

NGFF mSATA Conn



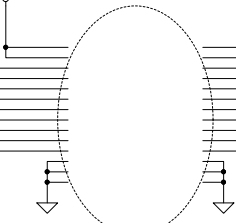
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[5] H_CPU_PWRGD
[5] XDP_TMS
[5] XDP_TDO
[5] XDP_TDI
[12] CPU_PWR_DEBUG
[5] XDP_PREQ#
[5] XDP_PRODY#
[15] CFG3
[10,9] SYS_RESET#

H_CPU_PWRGD
XDP_TMS
XDP_TDO
XDP_TDI
CPU_PWR_DEBUG
XDP_PREQ#
XDP_PRODY#
CFG3
SYS_RESET#

+1.05VS

+3VALW_PCH



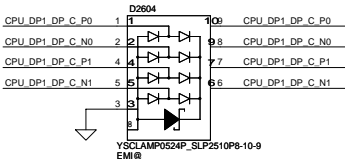
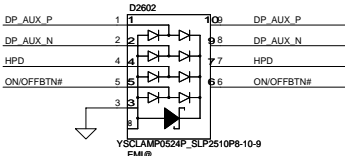
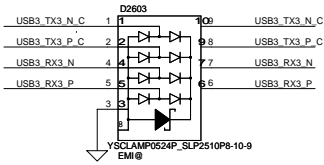
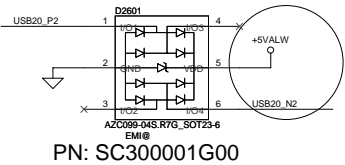
0815A

XDP_TCK
XDP_TRST#
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TMS
PCH_JTAG_TCK
PLT_RST_BUF#
SYS_PWROK
EC_RSMRST#

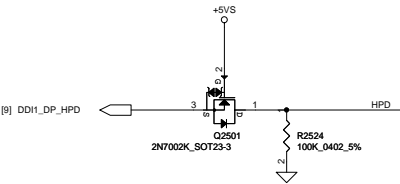
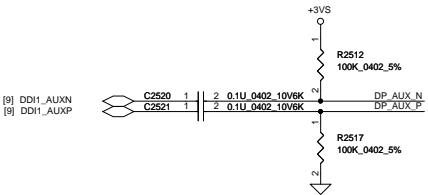
XDP_TCK [5]
XDP_TRST# [5]
PCH_JTAG_TDO [7]
PCH_JTAG_TDI [7]
PCH_JTAG_TMS [7]
PCH_JTAG_TCK [7]
PLT_RST_BUF# [21,22,27,30,31,8,9]
SYS_PWROK [31,9]
EC_RSMRST# [31,9]

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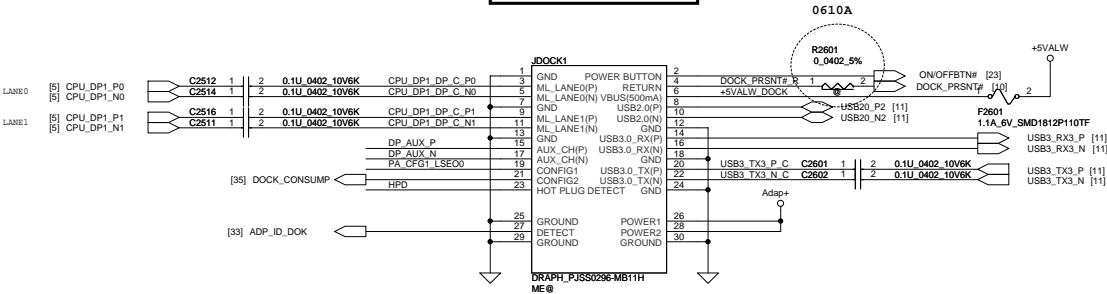
Docking (USB3.0)



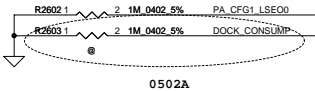
Docking (Display Port)



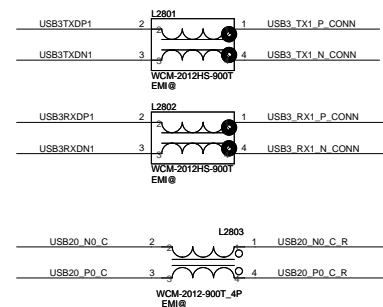
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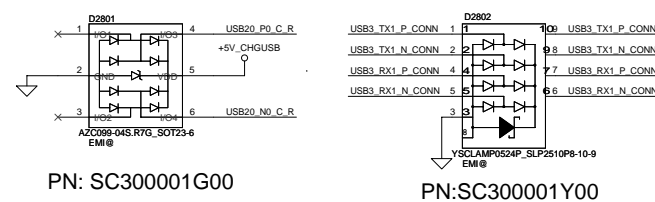
Footprint: DRAPH_PJSS0296-MB11H_24P-T



PN: SM070001S00 x 2



PN: SM070000K00 x 1



The diagram shows the internal connections of the PS8713BTOFN24GTR2_TQFN24_4XX4 package. It includes a central chip area with various pins and internal components like resistors (R2805, R2806, R2807, R2808, R2809, R2810, R2811, R2812) and capacitors (C2806, C2807, C2808, C2809). The package is connected to a +3VS supply and a GND. The internal connections are detailed with labels like CPU RX, CONN TX, and various pin numbers (1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24).

Pin Definitions:

- Pin 1:** A_EQ1
- Pin 2:** A_DE0
- Pin 3:** A_EQ0
- Pin 4:** A_DE1
- Pin 5:** A_EQ1/SDA_CTL
- Pin 6:** A_DE0/SCL_CTL
- Pin 7:** A_EQ0/INC
- Pin 8:** A_DE1/INC
- Pin 9:** A_Inp
- Pin 10:** A_InN
- Pin 11:** USB3RDXP1
- Pin 12:** USB3RDXN1
- Pin 13:** B_EQ1
- Pin 14:** B_DE0
- Pin 15:** B_EQ0
- Pin 16:** B_DE1
- Pin 17:** B_EQ1/I2C_ADDR1
- Pin 18:** B_DE0/I2C_ADDR0
- Pin 19:** B_EQ0/INC
- Pin 20:** B_DE1/INC
- Pin 21:** B_Outp
- Pin 22:** B_OutN
- Pin 23:** USB3TX1_P
- Pin 24:** USB3TX1_N

Component Values:

- Resistors:** R2805, R2806, R2807, R2808, R2809, R2810, R2811, R2812 (all 4.99K, 0402, 1%-D)
- Capacitors:** C2806, C2807, C2808, C2809 (all 0.1U, 0402, 10V6K)

Package Information: PS8713BTOFN24GTR2_TQFN24_4XX4

	A_EQ1/B_EQ1 (Internal pull Low)	A_EQ0/B_EQ0 (Internal pull Low)
reserved	Low	Low
program EQ for channel loss up to 7dB	Low	High
program EQ for channel loss up to 14.5dB	High	Low
program EQ for channel loss up to 11.5dB	High	High

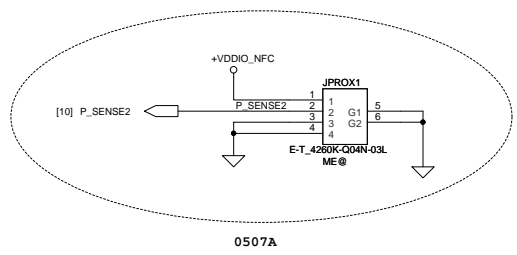
	A_DE1/B_DE1 (Internal pull Low)	A_DE0/B_DE0 (Internal pull Low)
3.5dB de-emphasis	Low	Low
No de-emphasis	Low	High
2.7dB de-emphasis	High	Low
5dB with boost output swing	High	High

	TEST (Internal pull Low)
Normal operation (default)	Low
Test mode enable	High

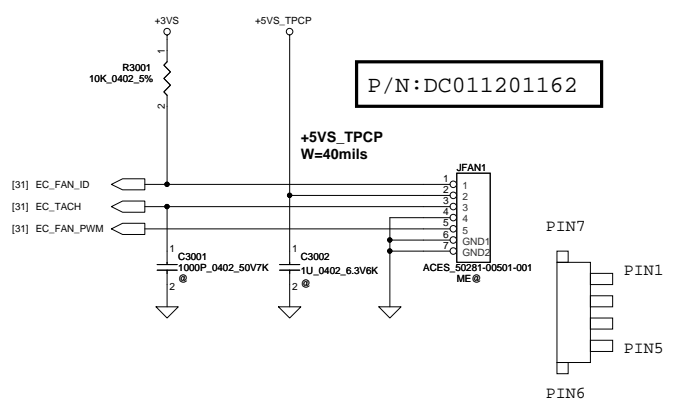
PN:SA000059H00

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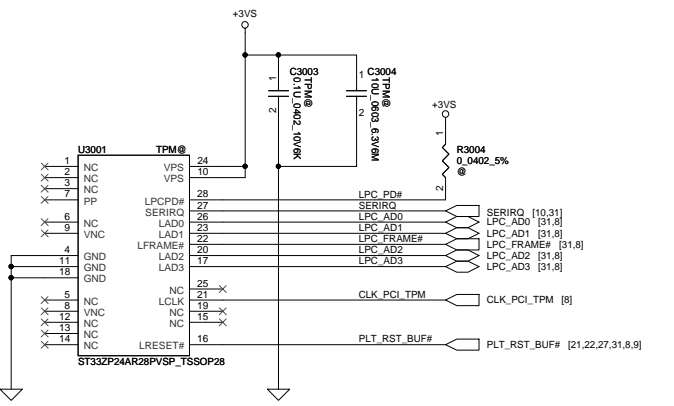
P-Sensor Conn



FAN Conn

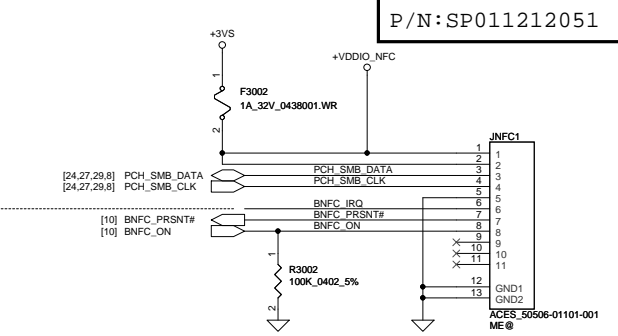
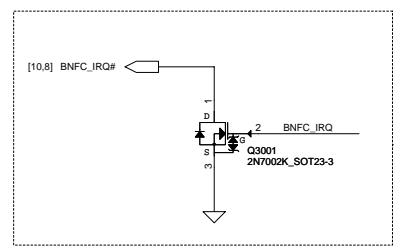


TPM



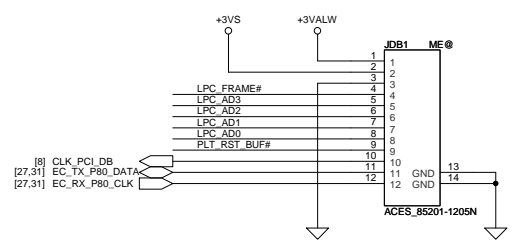
NFC

- Module Pin define
- 1.IP/VBAT
 - 2.IP/VDDIO
 - 3.IO/I2C-SDA
 - 4.I/I2C-SCL
 - 5.G/GND
 - 6.O/IRQ-NFC
 - 7.O/NFC_Presence#
 - 8.I/REG_UP
 - 9.OP/VDD_Ext_SE
 - 10.IP/UIM_PWR
 - 11.IO/SWP

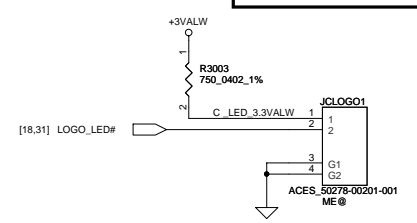


Conn

Debug Conn



C-logo Conn



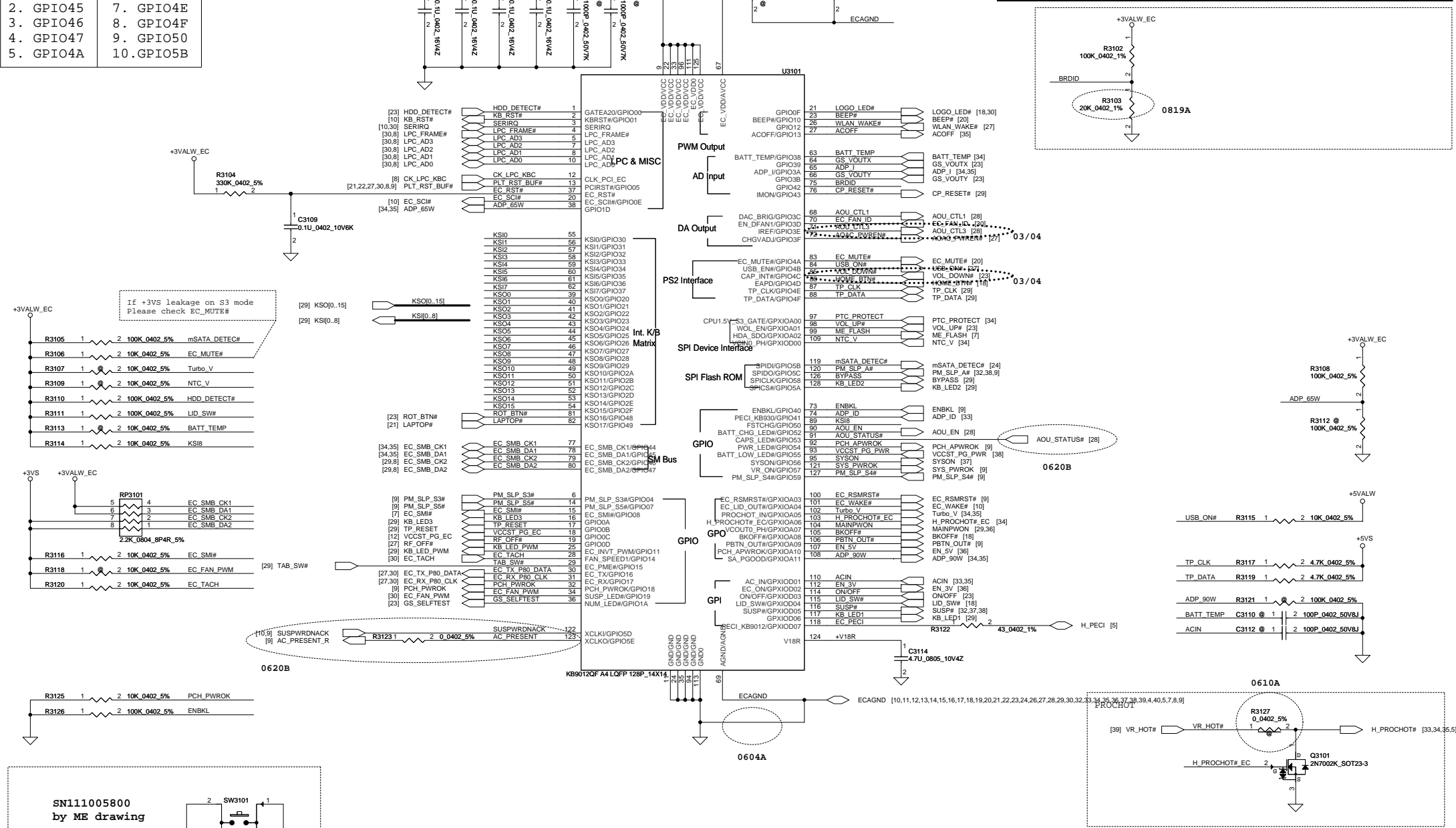
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EC KB9012

KB9012 A4 v.22

GPIO W/O internal-PH:

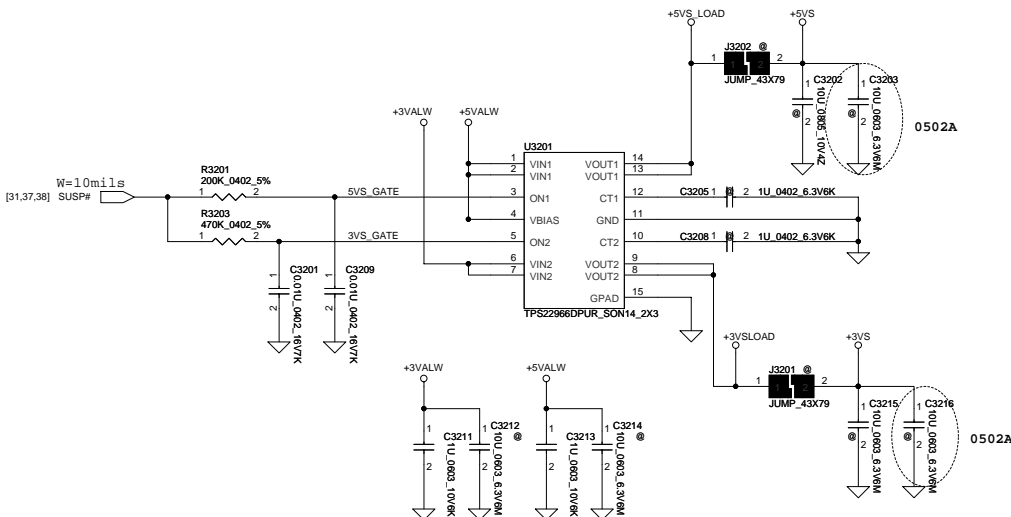
1. GPIO44	6. GPIO4B
2. GPIO45	7. GPIO4E
3. GPIO46	8. GPIO4F
4. GPIO47	9. GPIO50
5. GPIO4A	10. GPIO5B



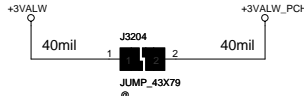
Vcc	3.3V +/- 5%				
R3102	100K +/- 1%				
Board ID	R3103	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD
SDV	0K +/- 5%		0.000V	0.300V	0x00 - 0x0B
FVT	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
SIT	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
SVT	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30

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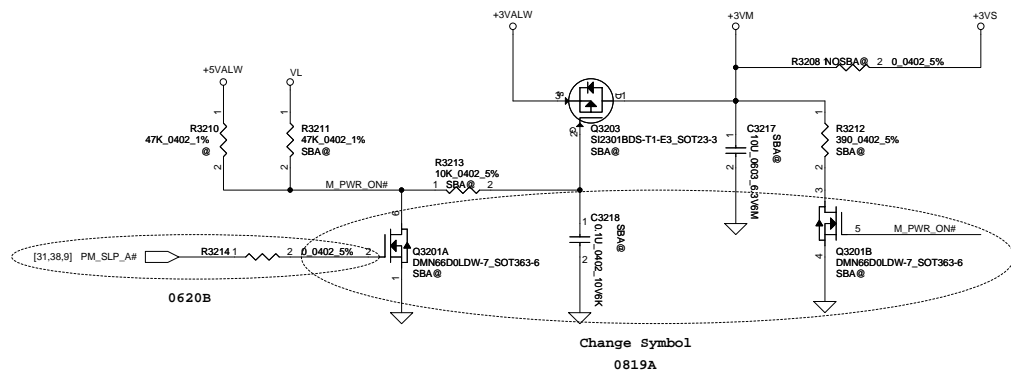
+5VALW TO +5VS
+3VALW TO +3VS



+3VALW TO +3VALW(PCH AUX Power)

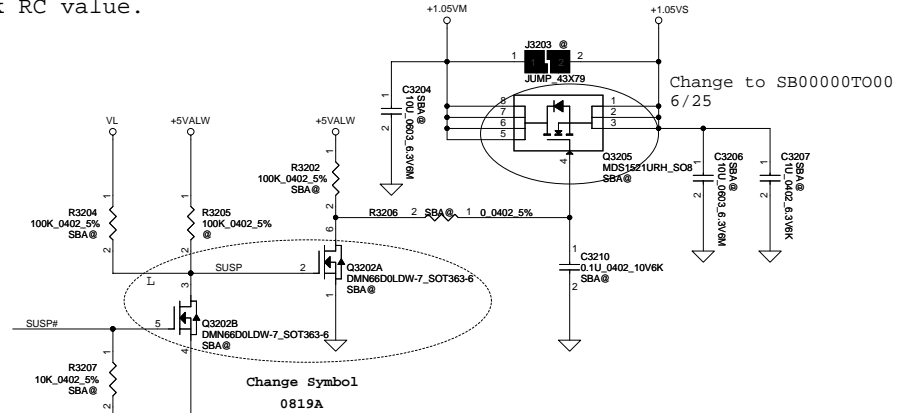


+3VALW TO +3VM (SBA)



PJ703 Short => NOSBA
PJ703 Open => SBA

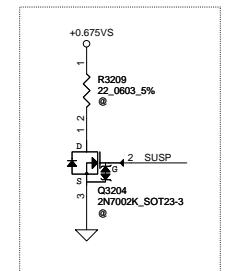
Check RC value.



DC/DC I/F

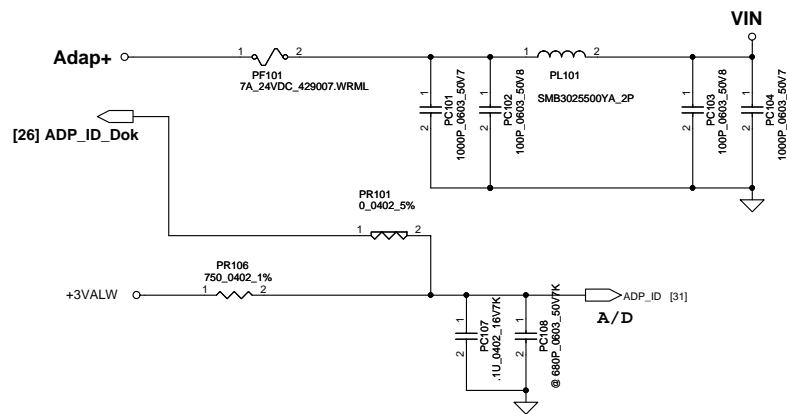
Rds(on) VGS=4.5V, ID=8.5A, 7mOhm(Max)

Change to SB00000T000
6/25

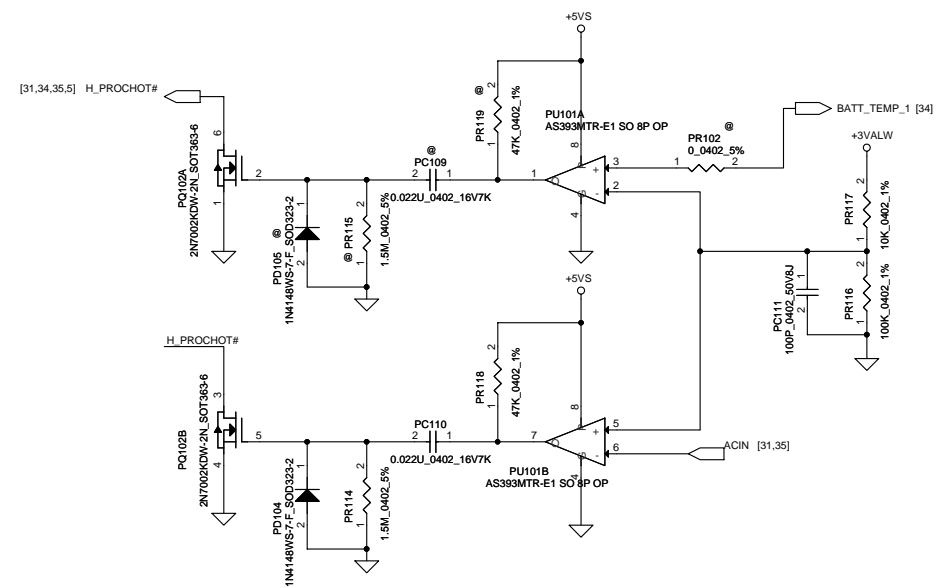
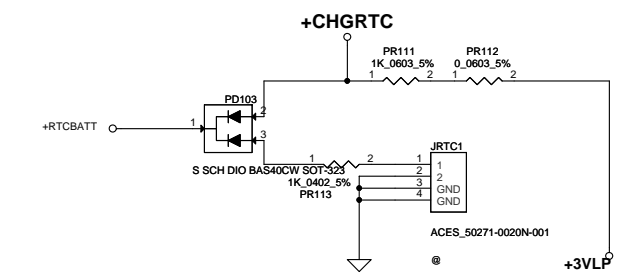


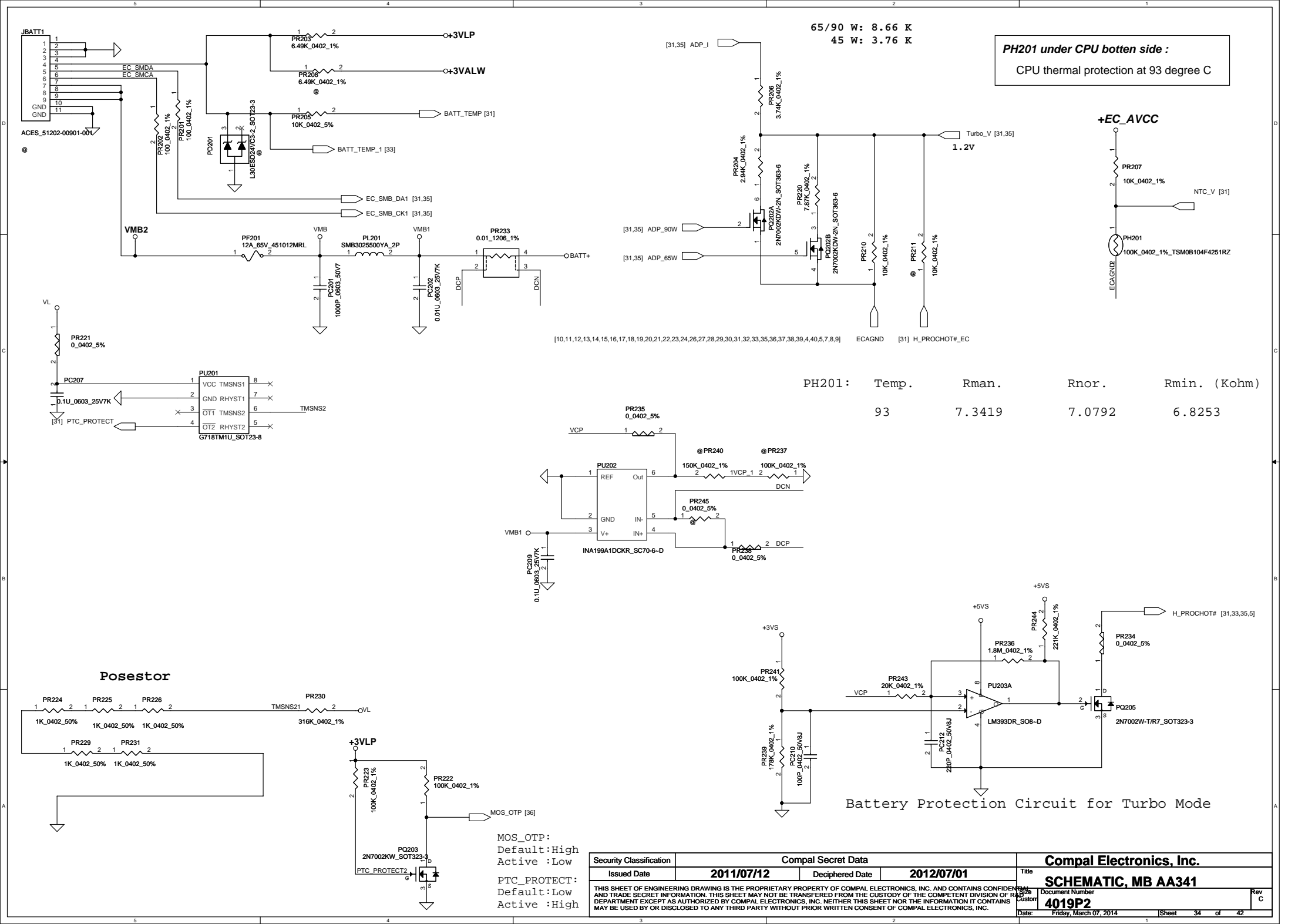
For Intel S3 Power Reduction

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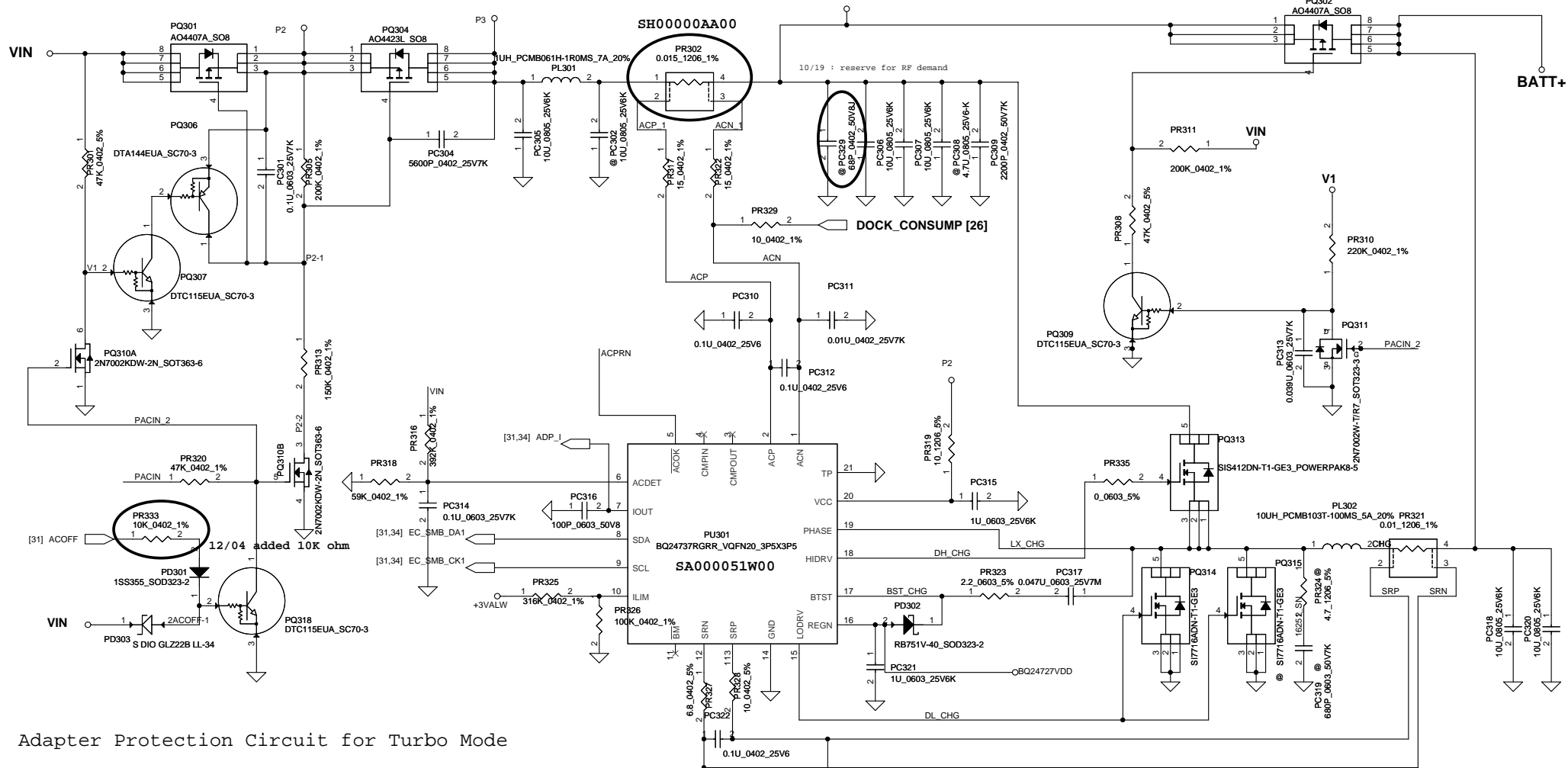


ADP_ID				
AC Adapter	45W	65W	90W	
R(ohm)	118	287	549	
ADP_ID(V)	0.449	0.913	1.395	
Detection	<=0.663,			<=1.134,
-Voltage(V)	>0.234			>0.693
				>1.172

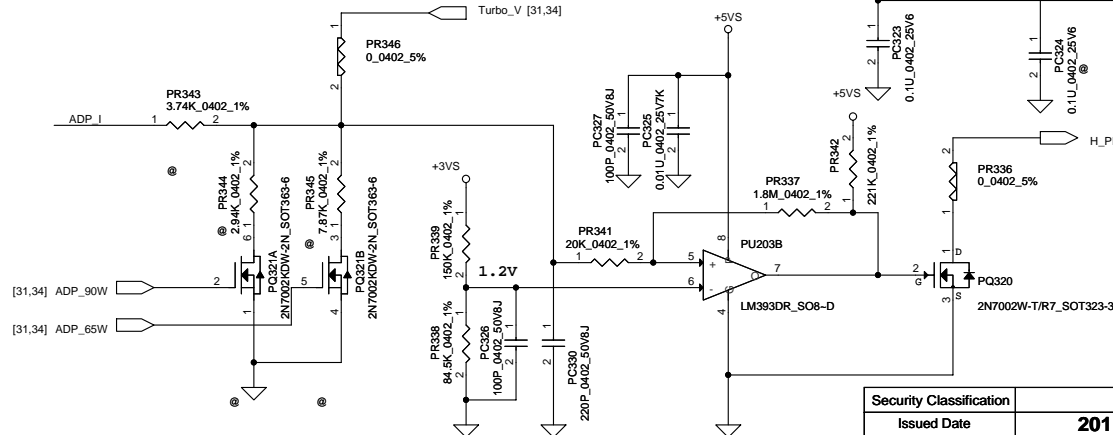




DCR 换成 15m ohm,CP,Throttling....need redefine with EC

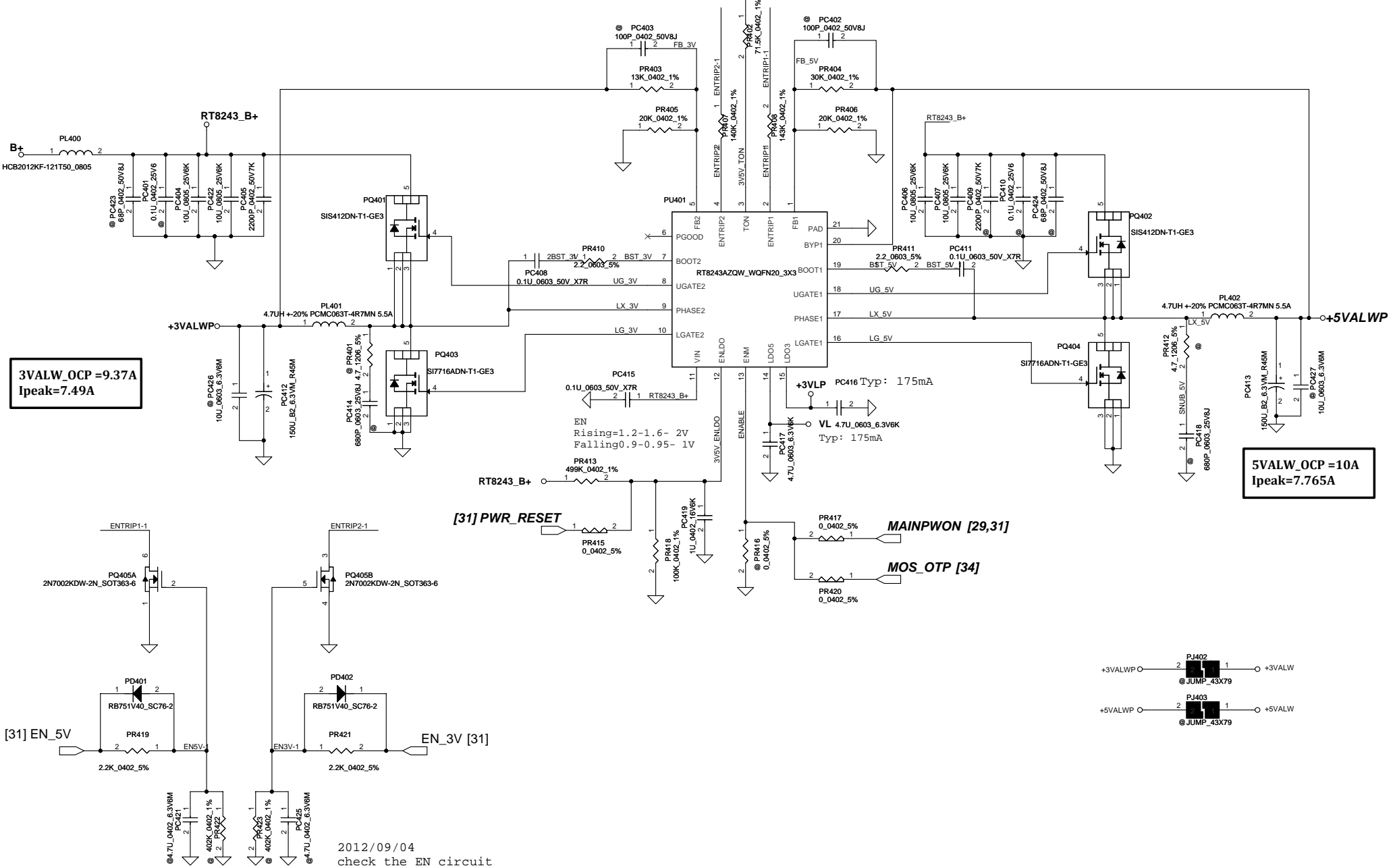


Adapter Protection Circuit for Turbo Mode



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TON (1)SMPS1=305KHZ (+5VALWP)
(2)SMPS2=357KHZ(+3VALWP)



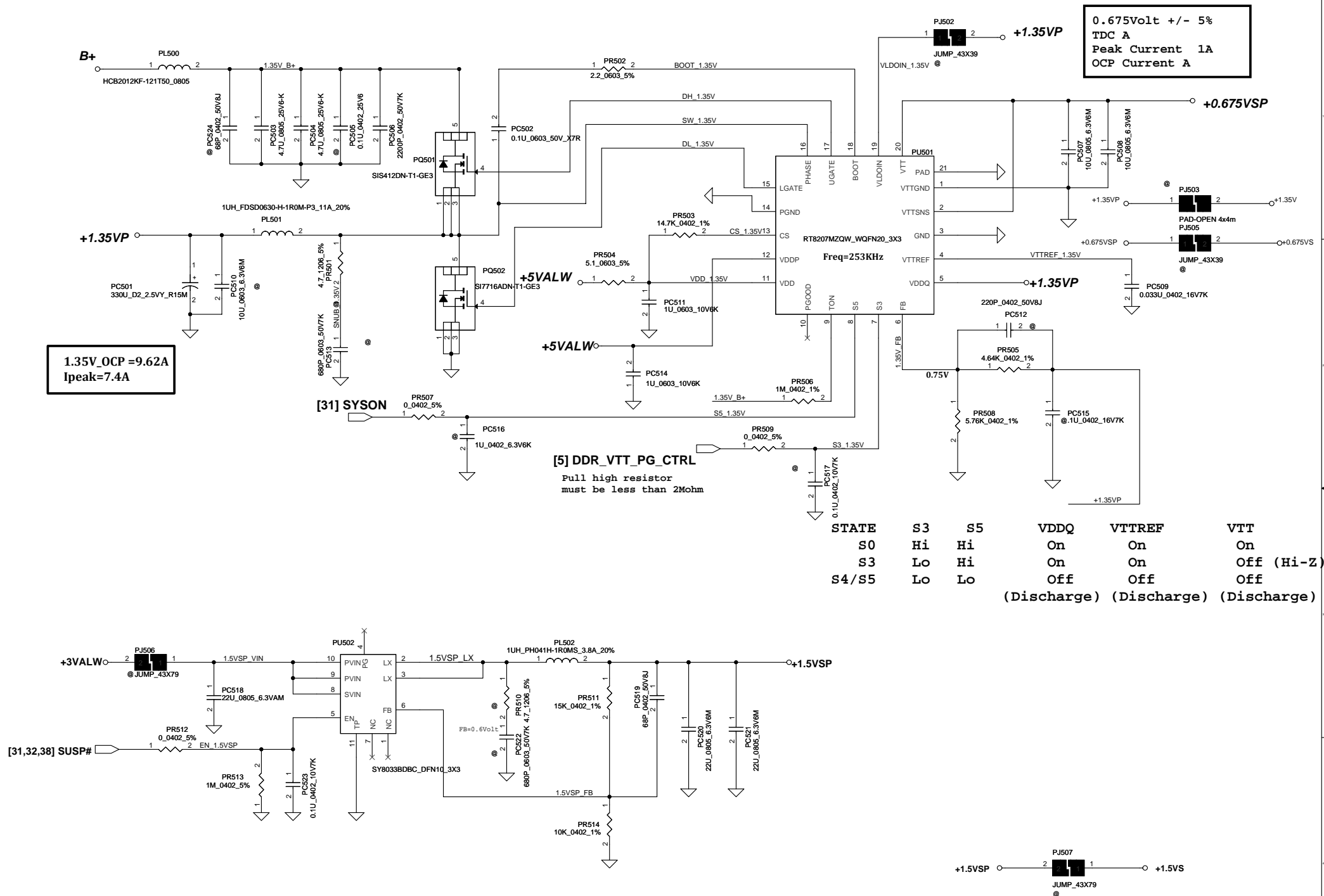
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Ipeak=7.49A

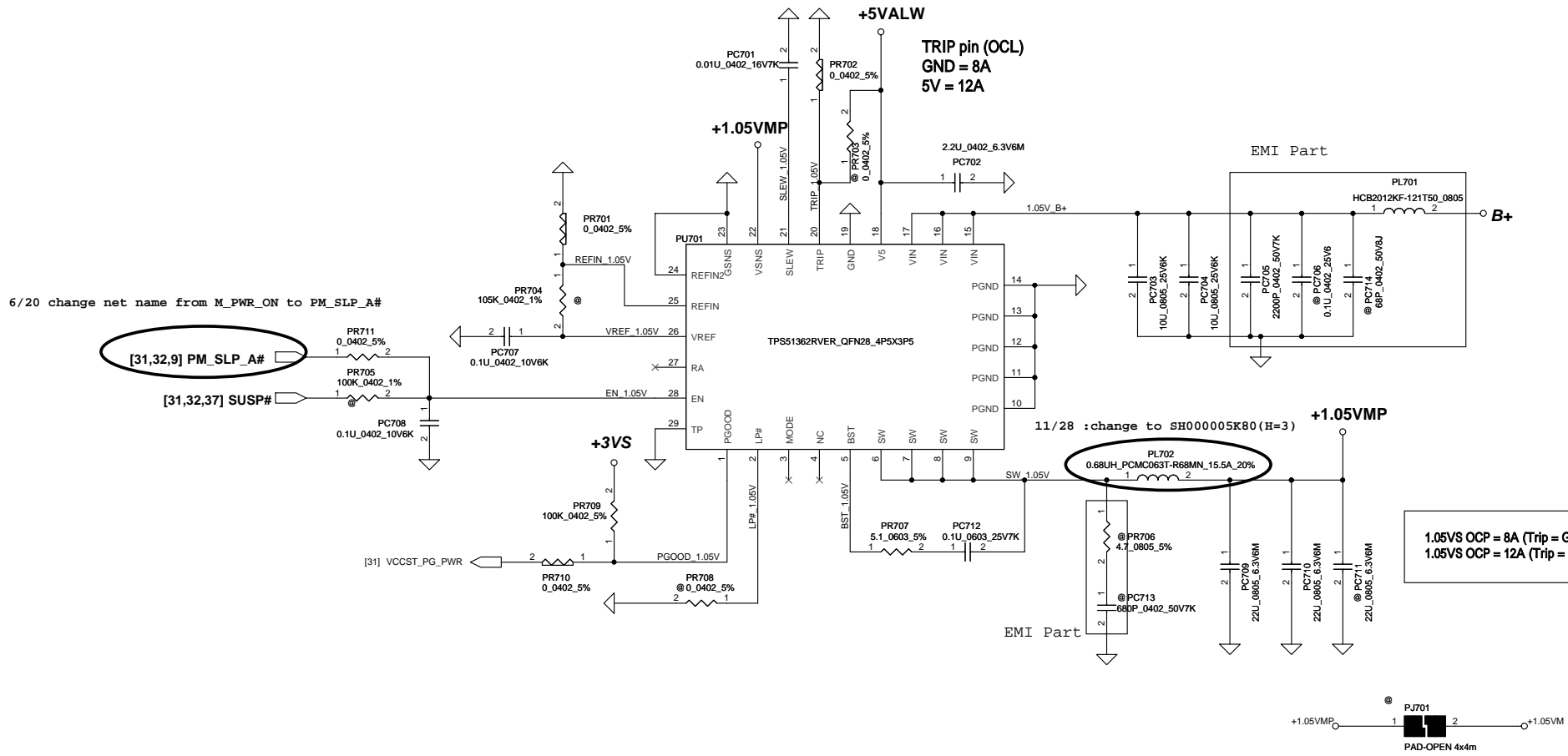
5VALW_OCP=10A
Ipeak=7.765A

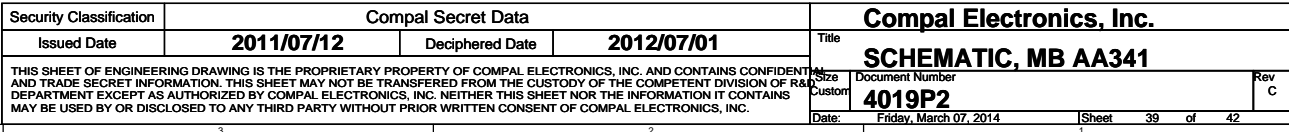
[31] EN_5V
[31] EN_3V [31]

2012/09/04
check the EN circuit

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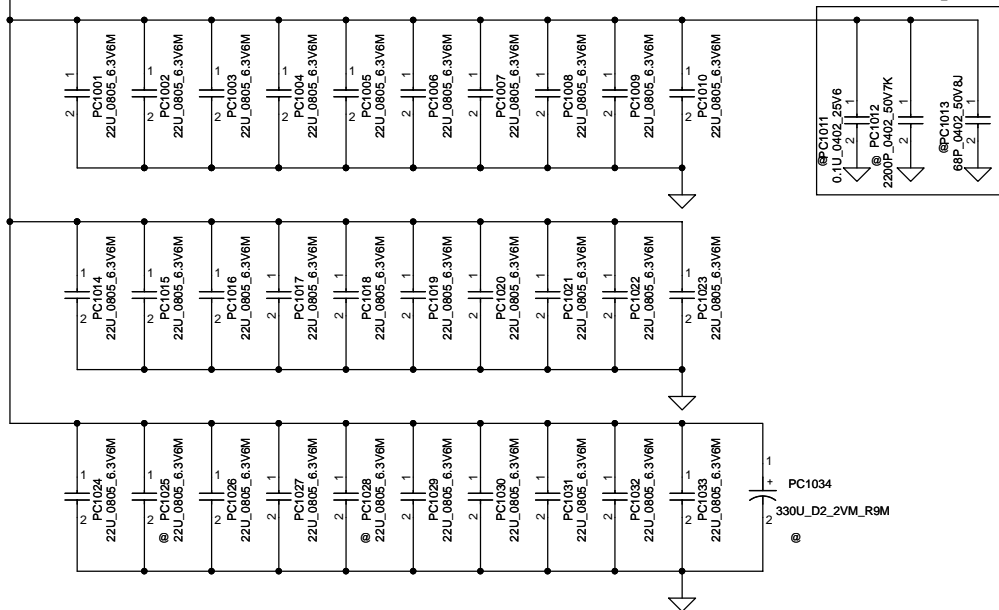




+CPU_CORE

30 X 22u/0805

RF request



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Item	Reason for change	PG#	Modify List	Date	Phase
1	We just have adpter over-load protection circuit to replace the one-shot circuit, so we can reserve the one-shot circuit.	P33	Un-mount PR119, PC109, PR115, PD105.	2013.04.24	SDV
2	We want to tune the switching ring to meet the derating spec.	P37	Change PC502 from 0.22u to 0.1u.	2013.04.24	SDV
3	For fine tune LL & trainsient of CPU core, we must to change R/C value to meet Intel's spec.	P39	Change PR916 from 47k to 73.2k and PC923 from 560p to 100p, PC1025, PC1028, PC1034 to un-mount.	2013.04.24	SDV
4	For aviod EMI/EMI to damage OP or other components through the loop of BATT_TEMP.	P34	Reserve PD201	2013.04.30	SDV
5					
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Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function

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		Custom		Rev C	
Date		Friday, March 07, 2014		Sheet	42 of 42